BEN GRAS/@BJG, KAVEH RAZAVI, CRISTIANO GIUFFRIDA, HERBERT BOS
VRIJE UNIVERSITEIT AMSTERDAM

BLACKHAT USA 2018

SPYING ON YOUR NEIGHBOR: CPU CACHE ATTACKS AND BEYOND

ABOUT ME

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- PhD student in VUsec VU University Research group

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- Academic group researching systems software security

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OVERVIEW

- Side channels
- Cache attacks
- Cache defences
- Hyperthreading
- TLBleed
- Evaluation

SIDE CHANNELS

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- Leak secrets outside the regular interface

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RICH HISTORY - SMARTCARDS

- Power Consumption

  (FPGA Security by Shemal Shroff et al.)

- EM radiation: leak ECC bits

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- Execution time: leak ECC, RSA bits

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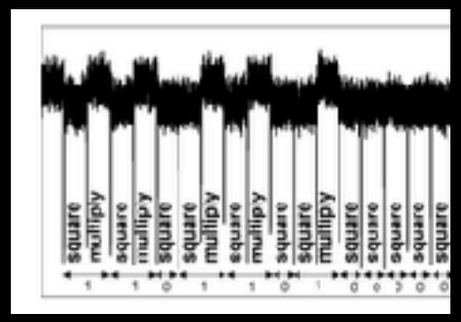

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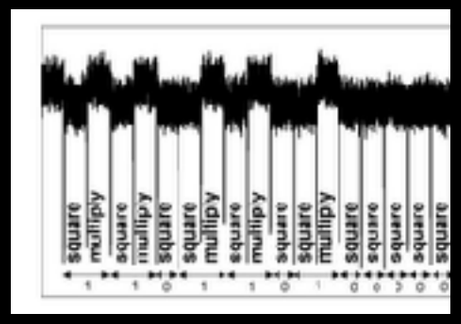

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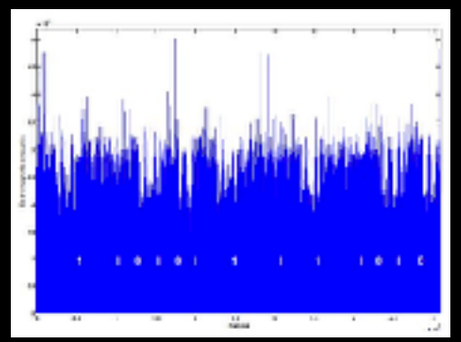

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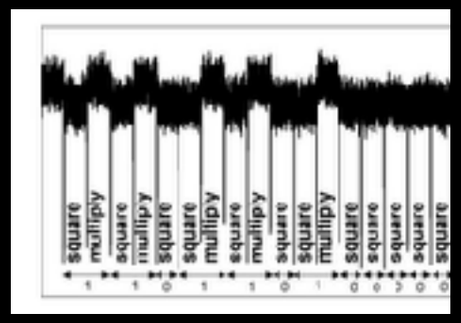

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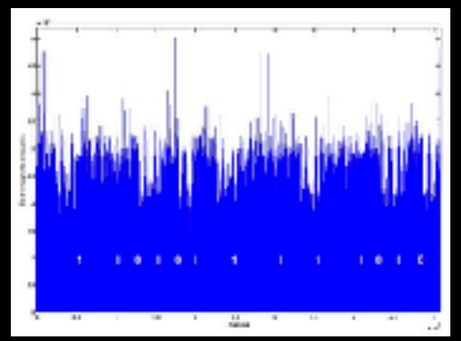

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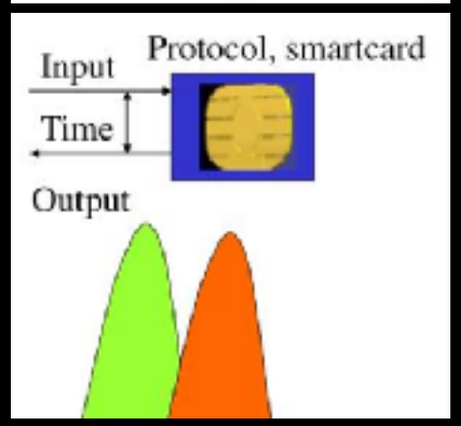

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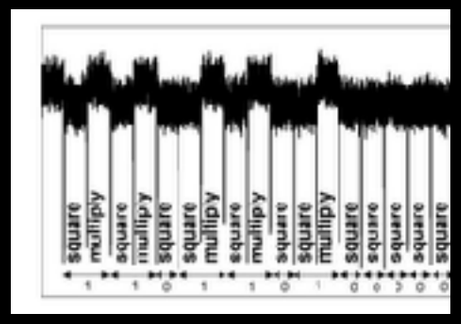

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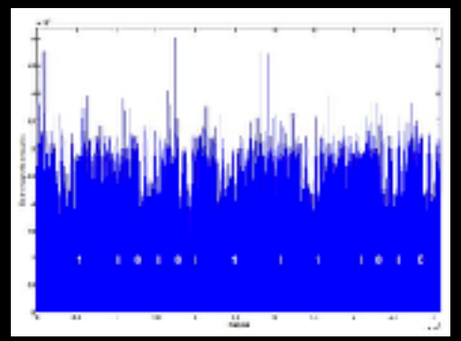

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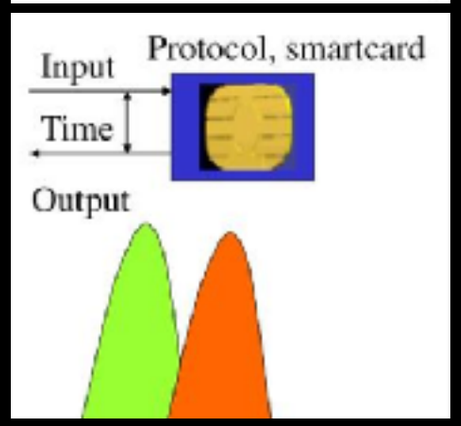

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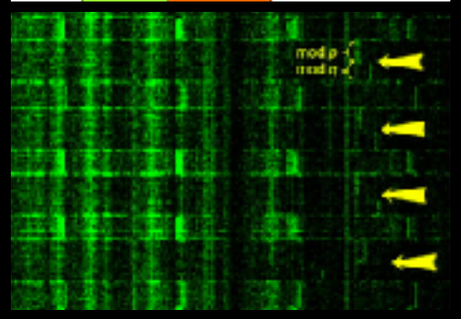

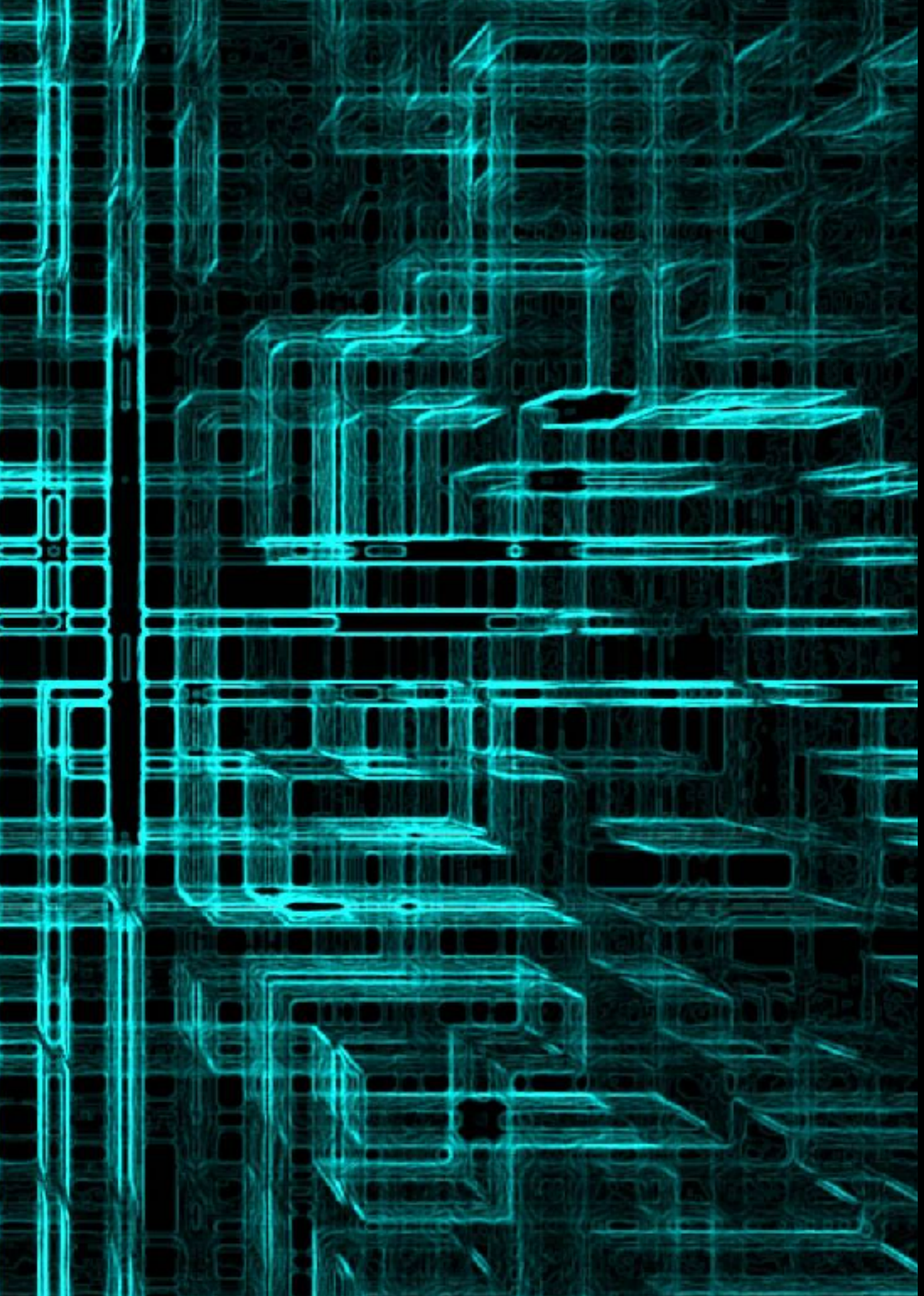

CACHE ATTACKS

CACHE: SOFTWARE EQUIVALENT

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- Different owners or privilege levels: *trust boundaries*

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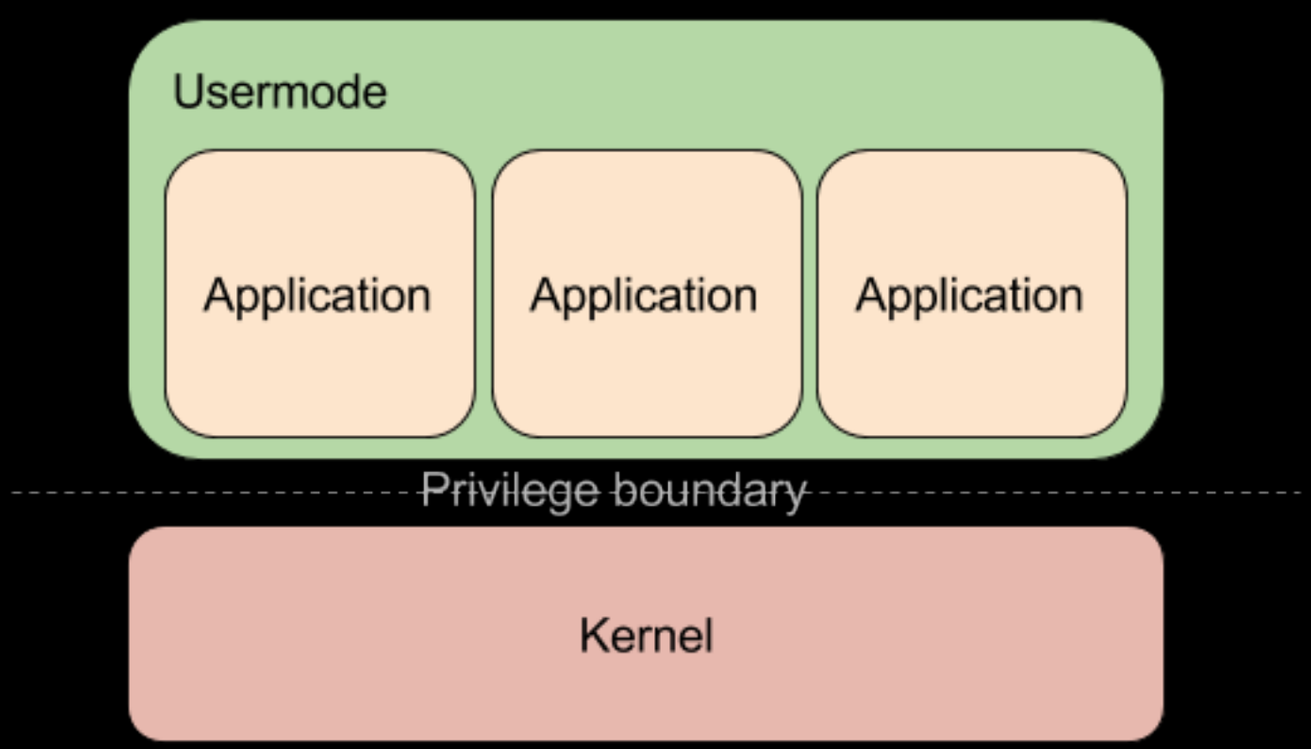

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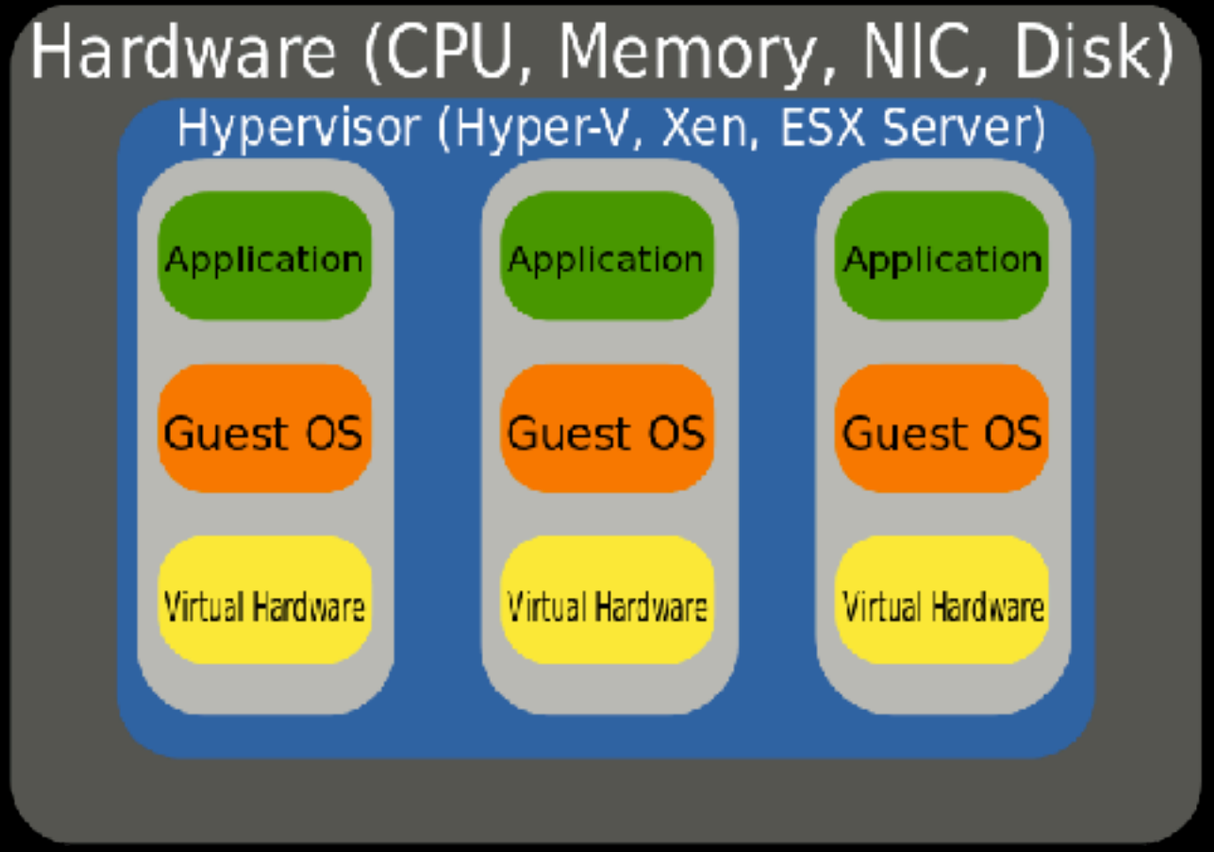

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CACHE: SOFTWARE EQUIVALENT

- There are **shared** resources between processes
- RAM, CPU cache, TLB, computational resources ..
- Practically always: allows signaling: covert channel
- Sometimes: allows side channel (spying)

CROSS-PROCESS SHARED STATE

- Shared RAM row
  (DRAMA paper, by Peter Peßl et al.)

- Shared cache set
  (FLUSH+RELOAD by Yuval Yarom et al.
  shown, many others exist)

- Cache prefetch
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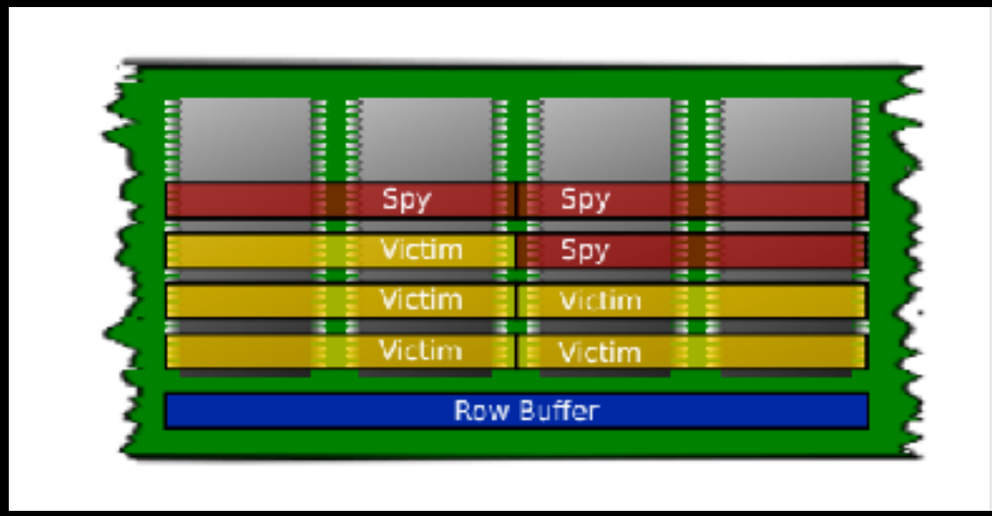

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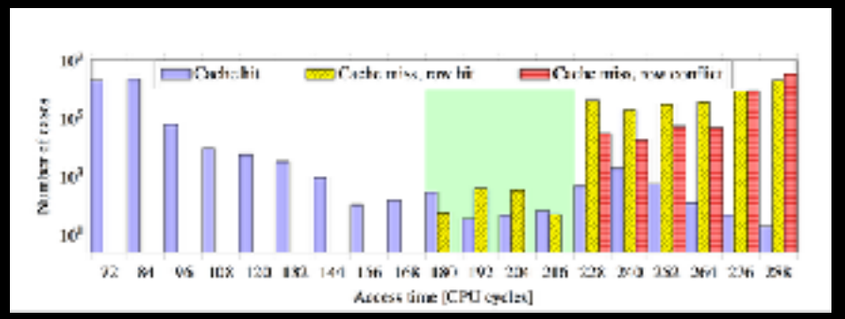

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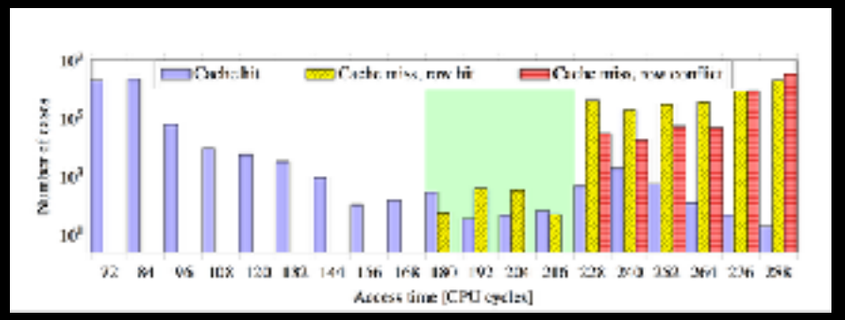

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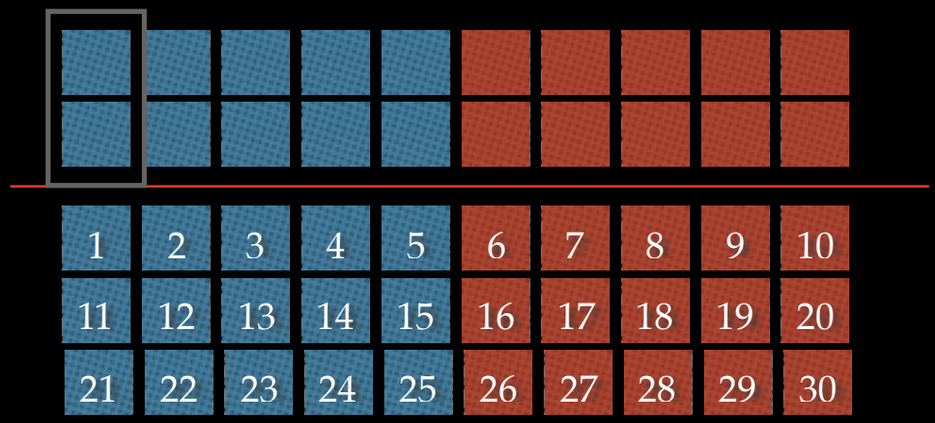

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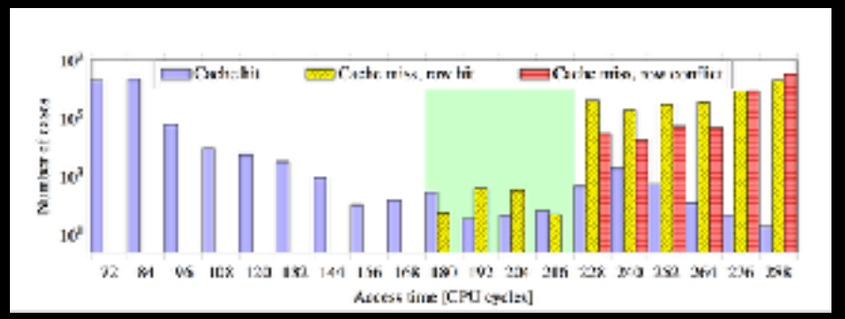

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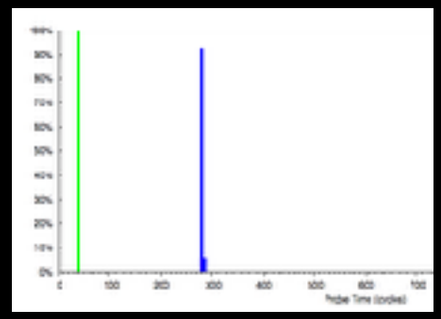

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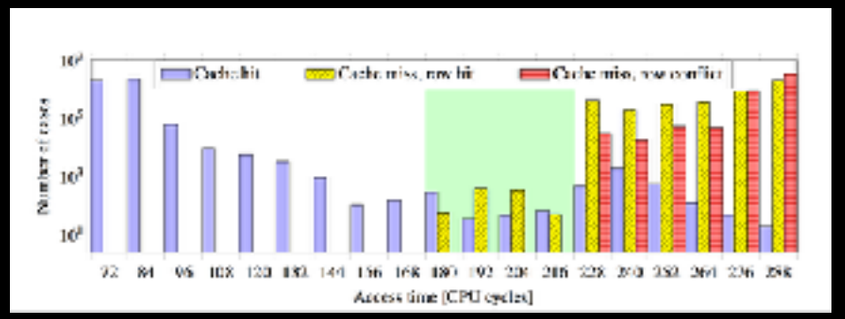

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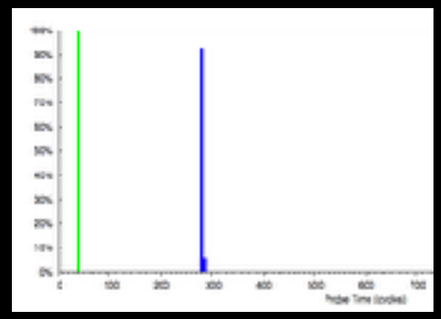

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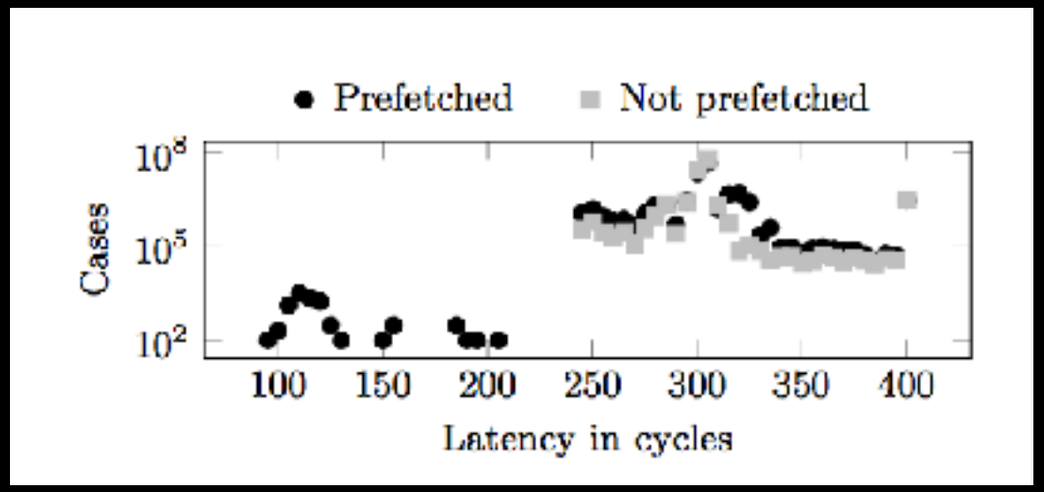

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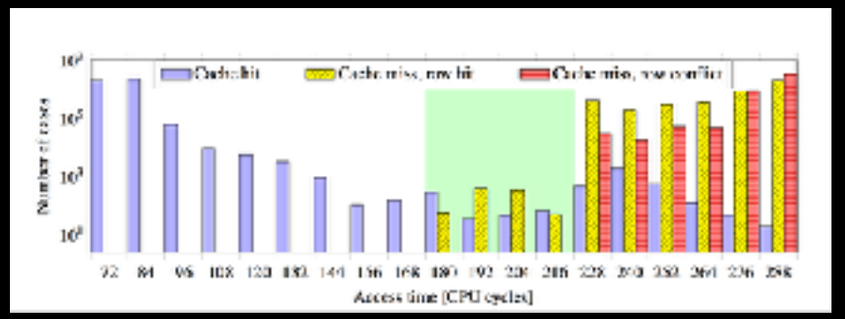

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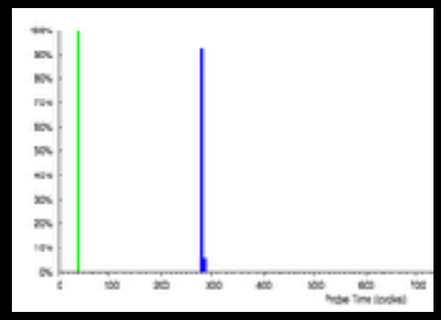

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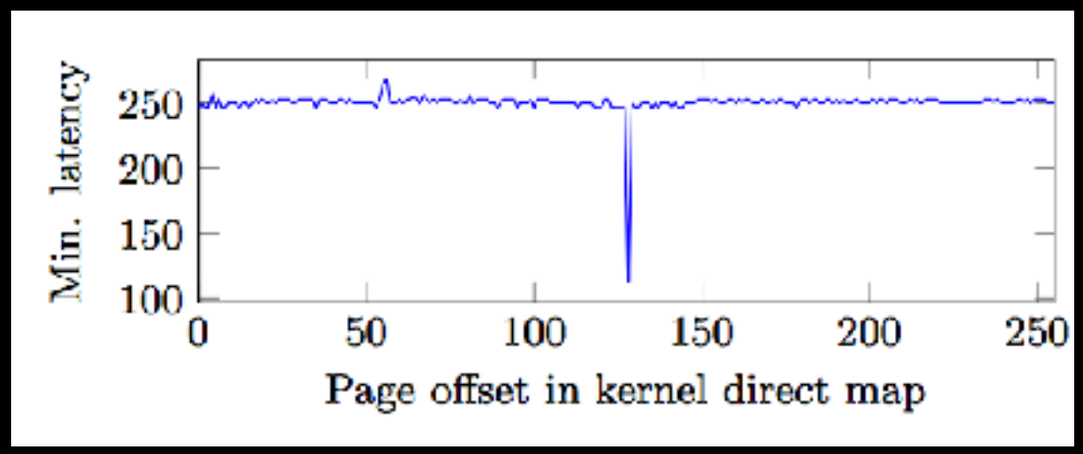

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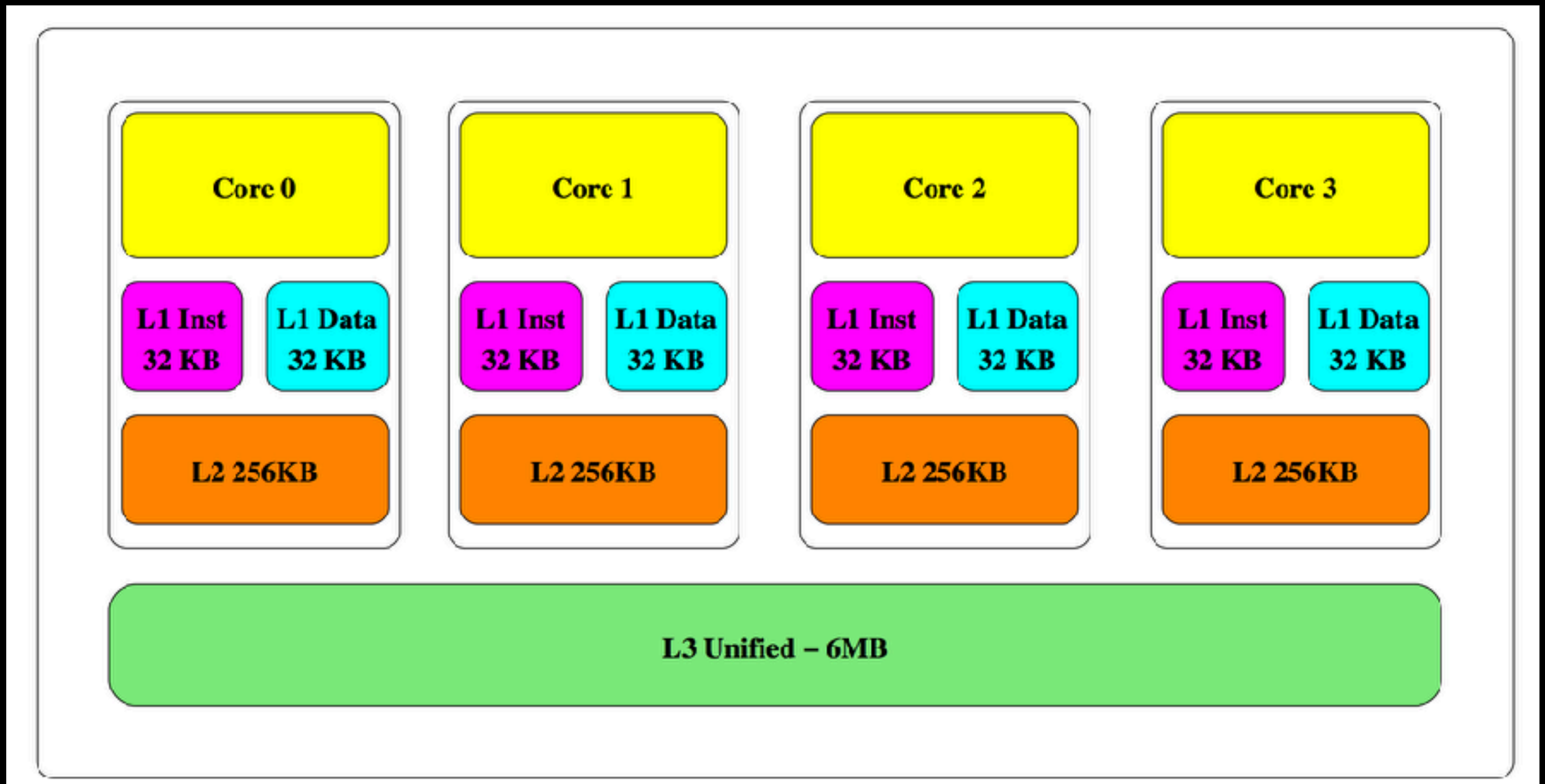

EXAMPLE: FLUSH+RELOAD

- One of several cache attacks
- Relies on shared memory
- Can be shared object (mmap()ed shared libraries)
- Or shared pages after deduplication (KSM in Linux)

EXAMPLE: FLUSH+RELOAD

- Work by Yuval Yarom, Katrina Falkner
- Memory access patterns can betray secrets
- Because access patterns frequently depend on secrets
- Example: RSA keys. *(n,e,d)* Private: *d*. *n=pq* and *d* are 1024 bits or more

EXAMPLE: FLUSH+RELOAD

- Signing is: computing $m^d \pmod n$
- Often square-and-multiply **depending on** bits in *d*

- Shared cache activity betrays memory access patterns
- Quickly probing the cache can betray the bits in *d*

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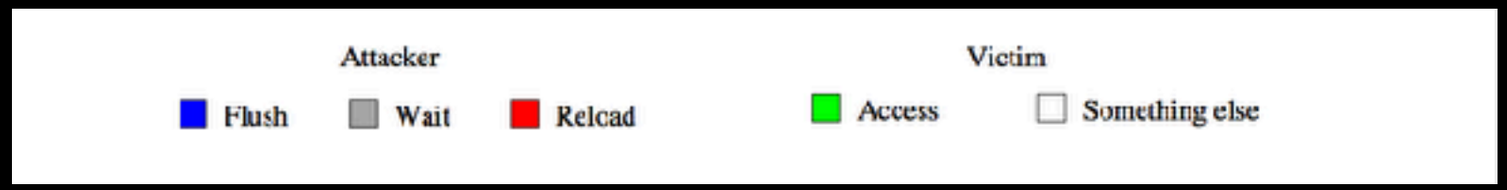

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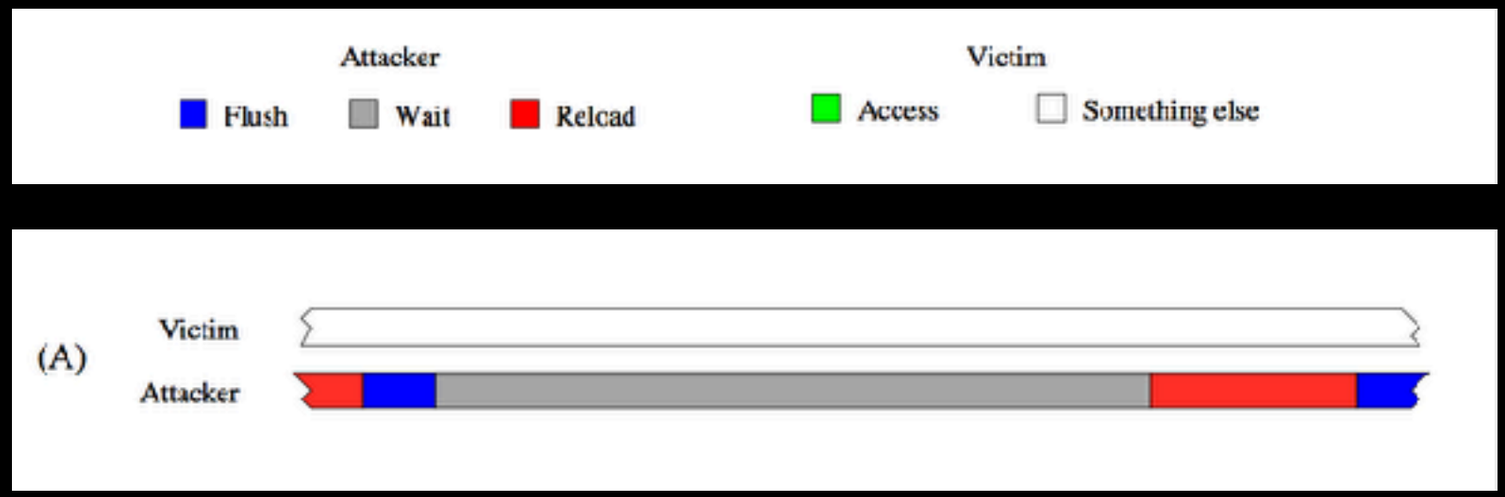

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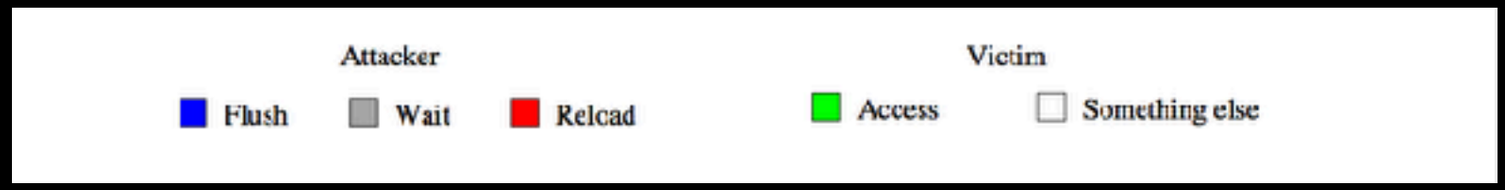

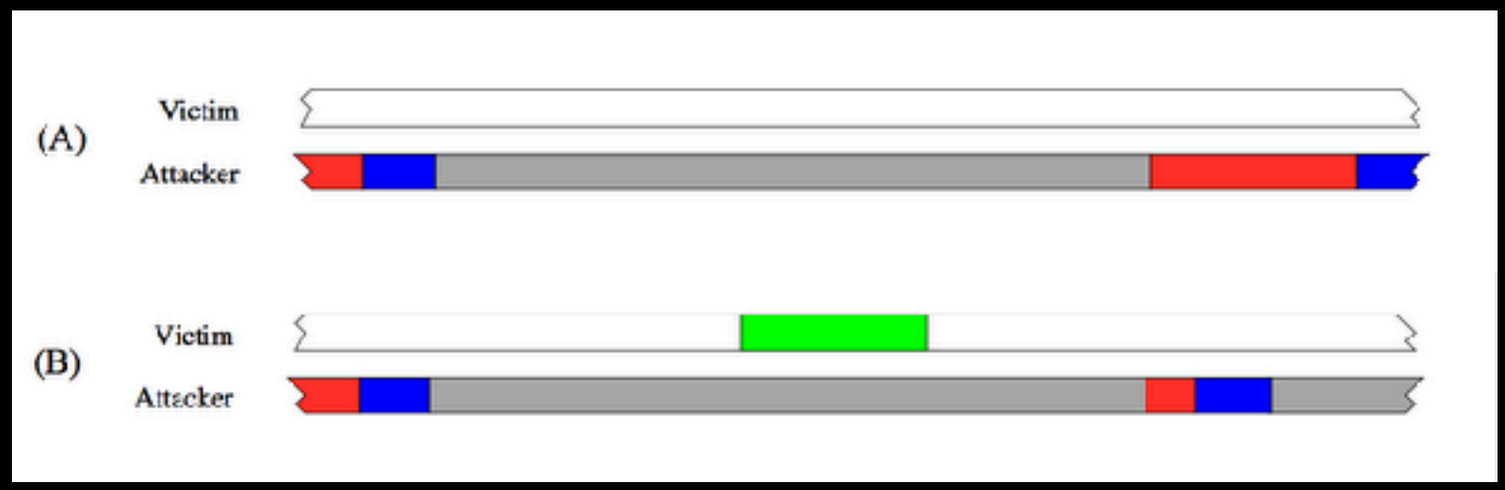

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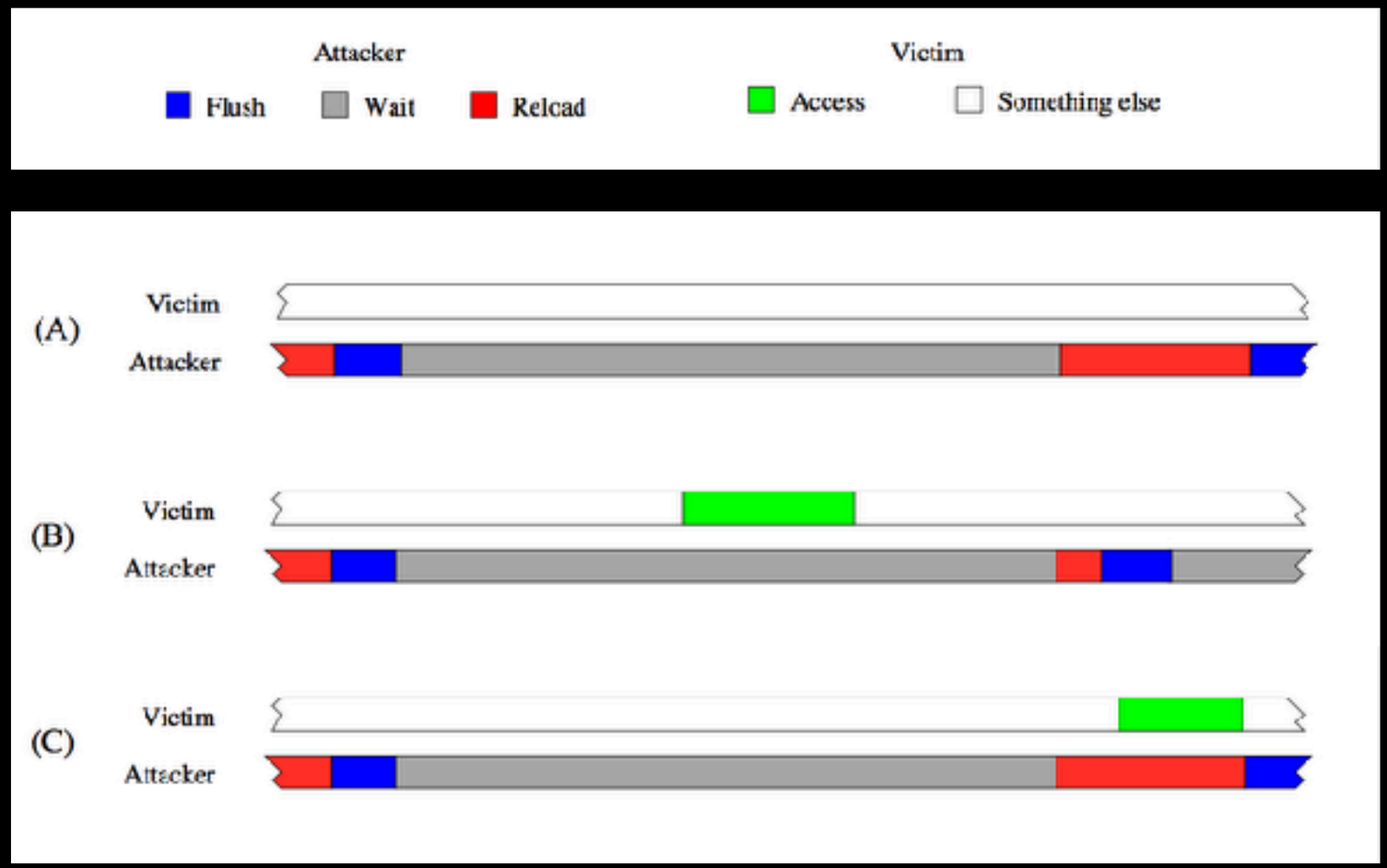

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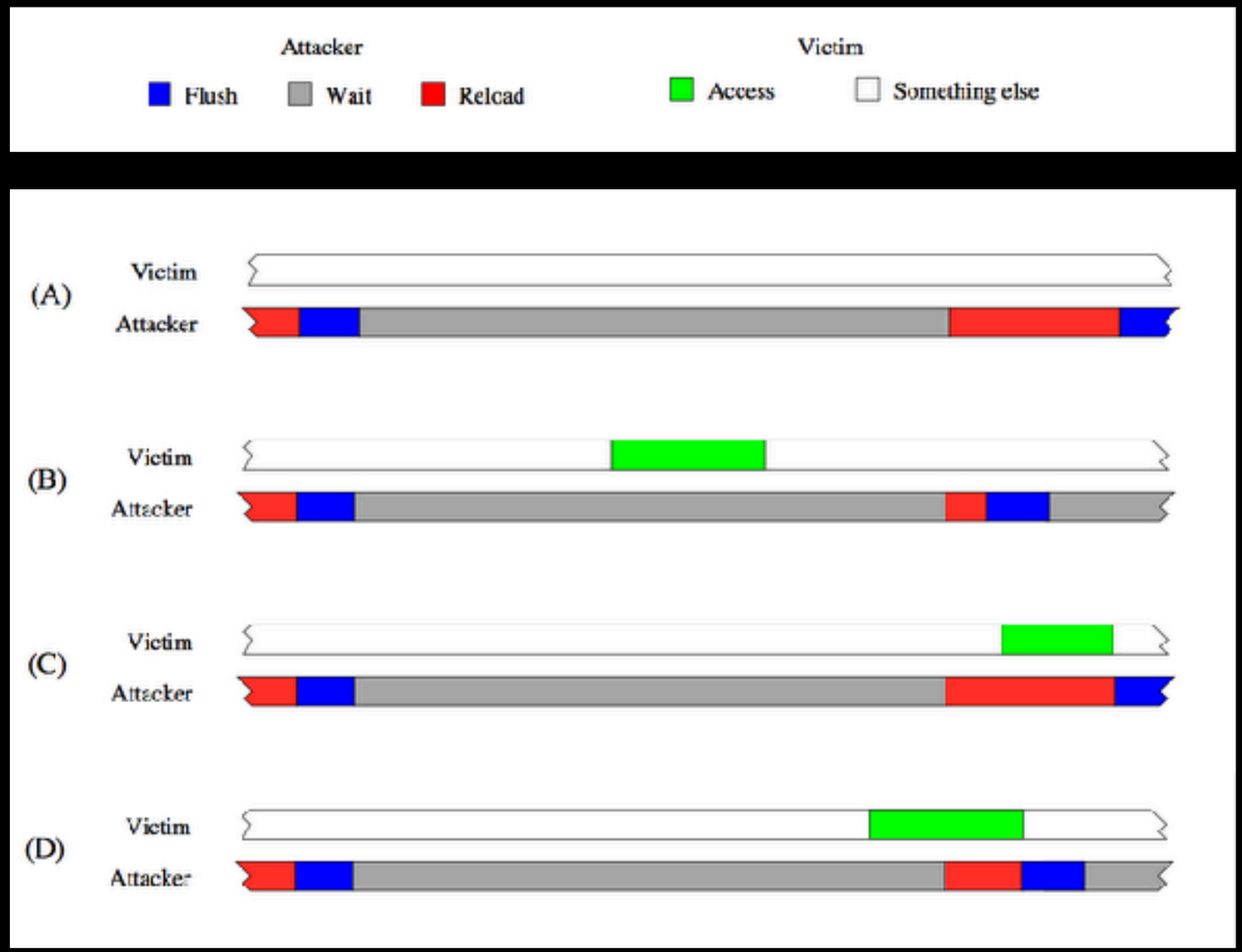

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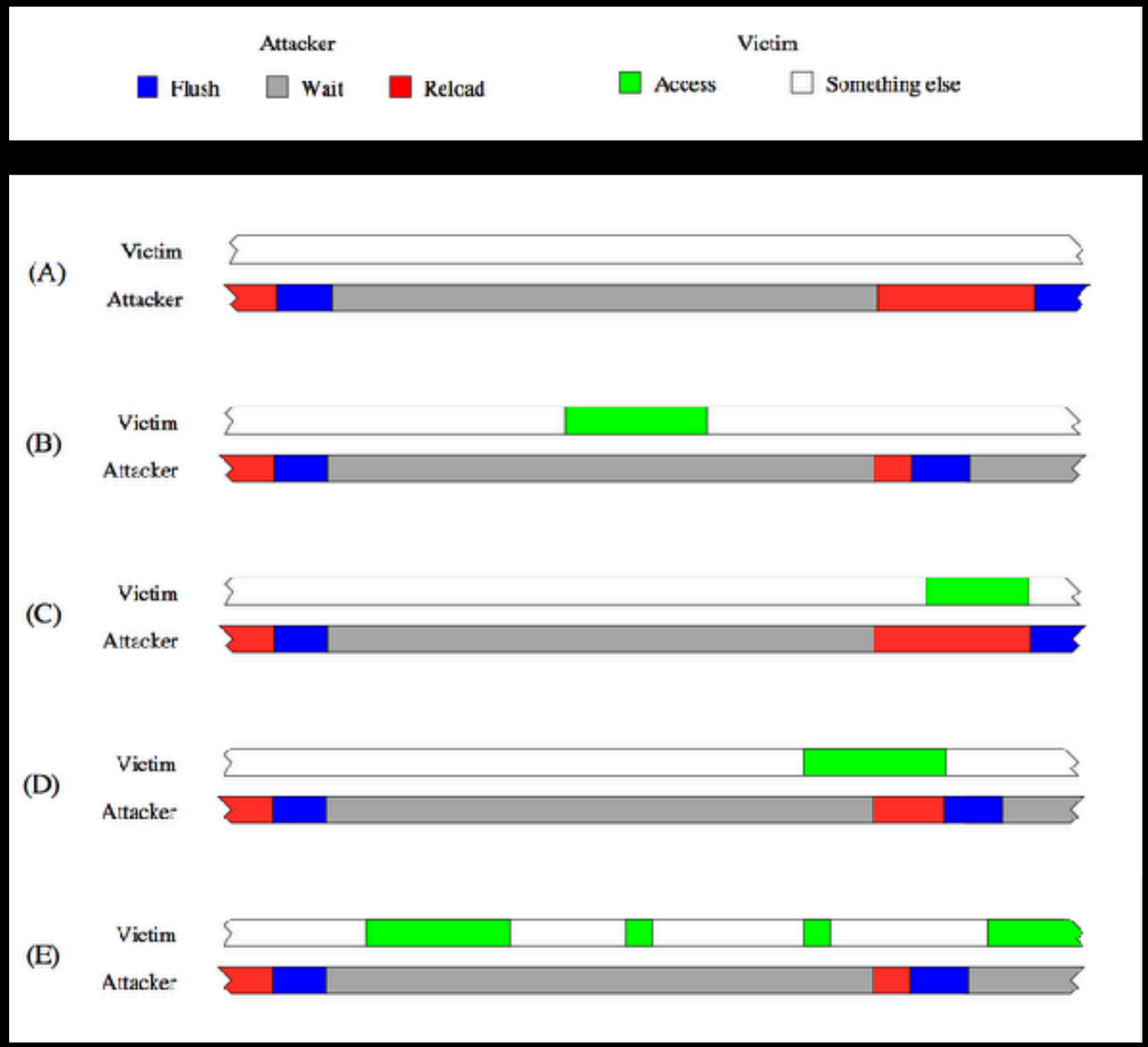

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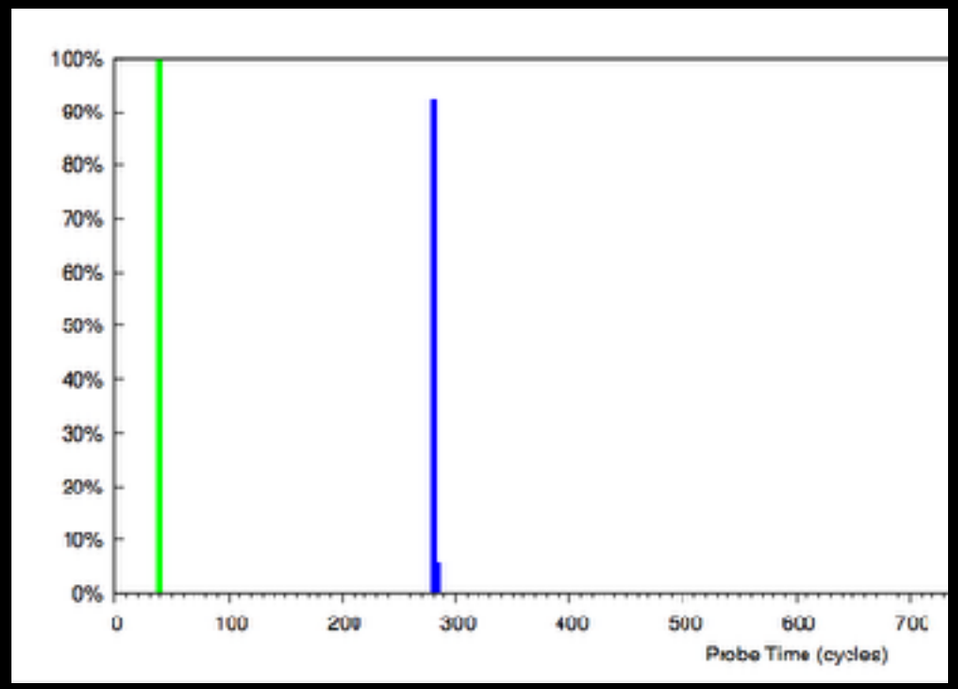

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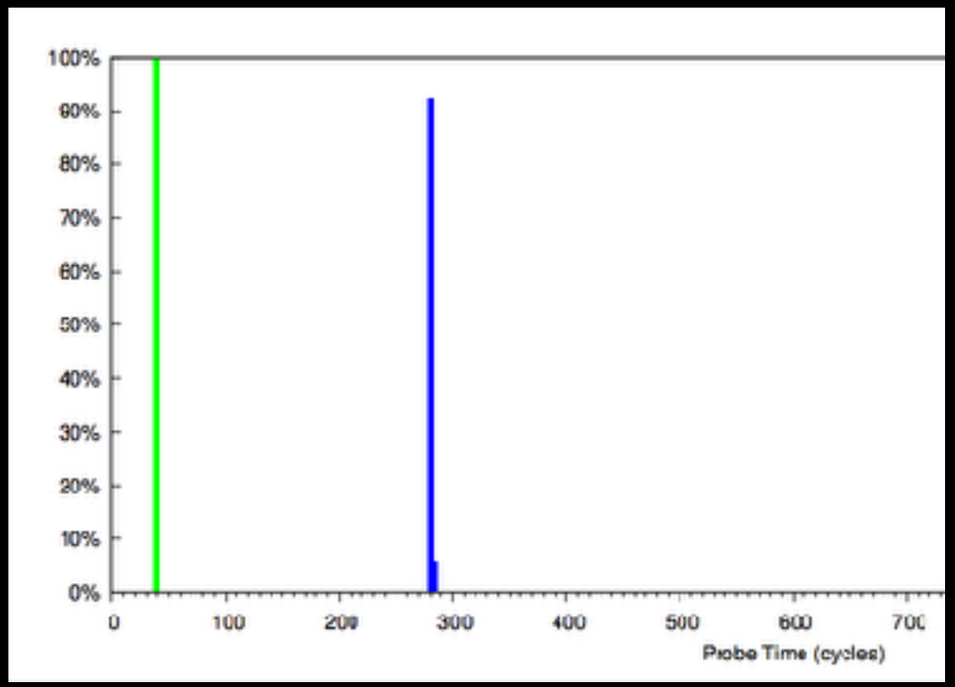

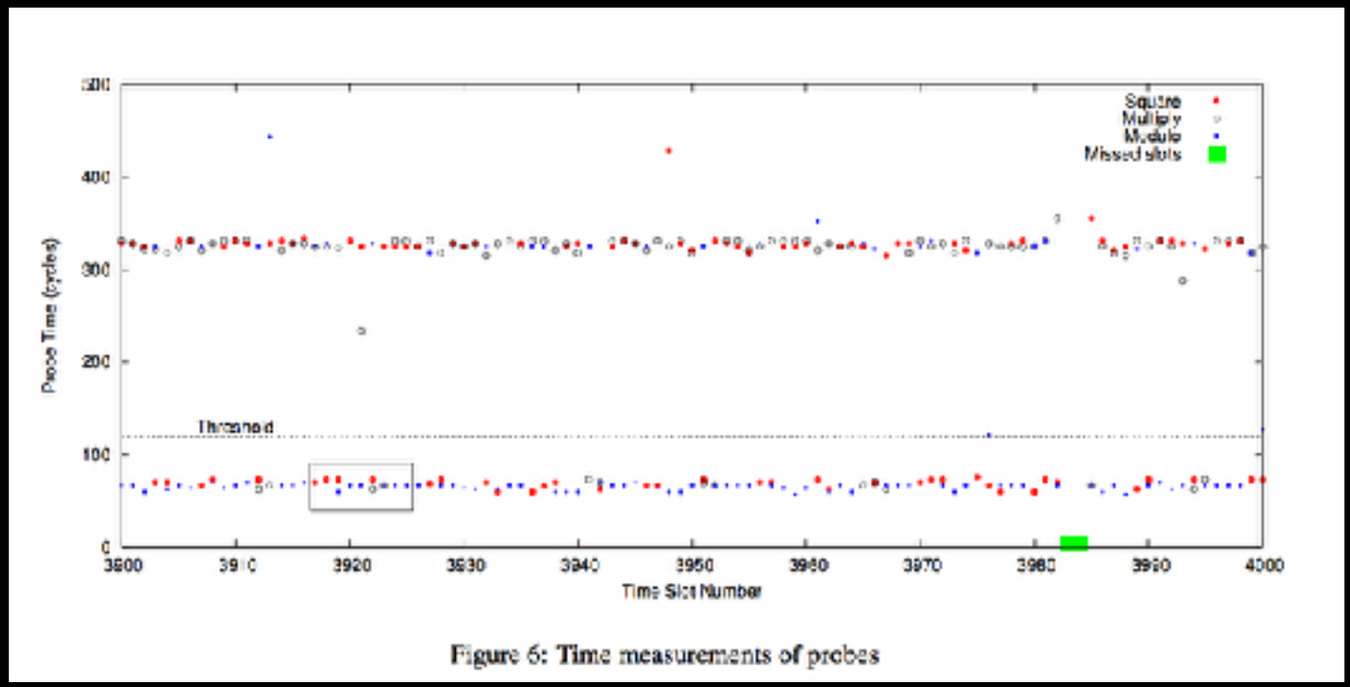

Figure 6: Time measurements of probes

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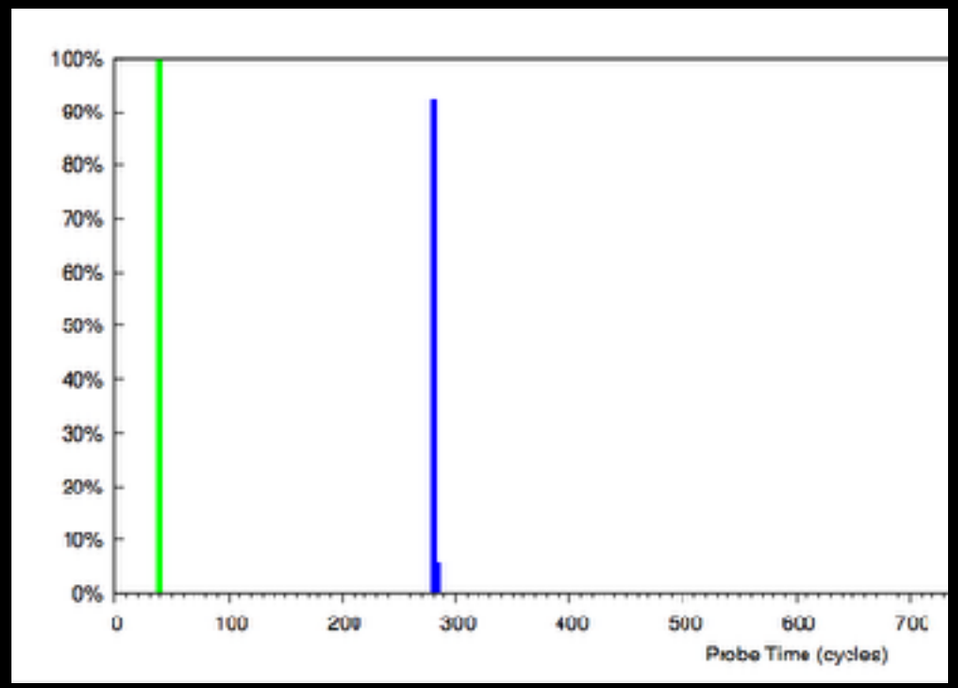

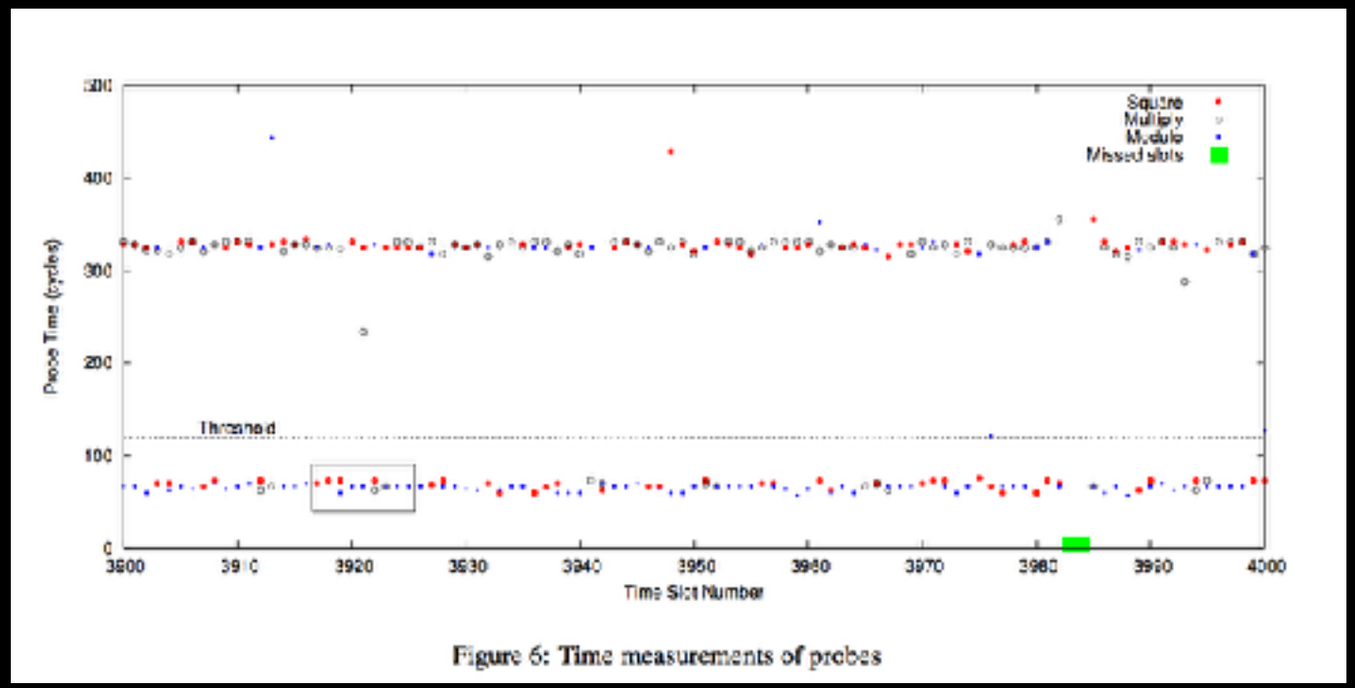

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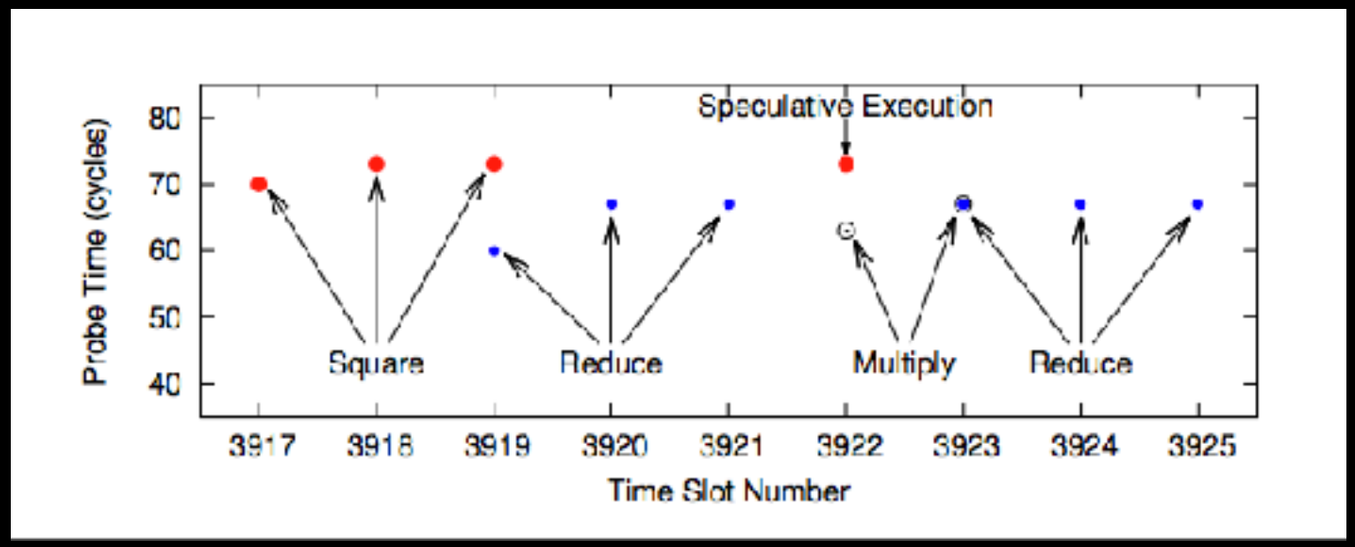

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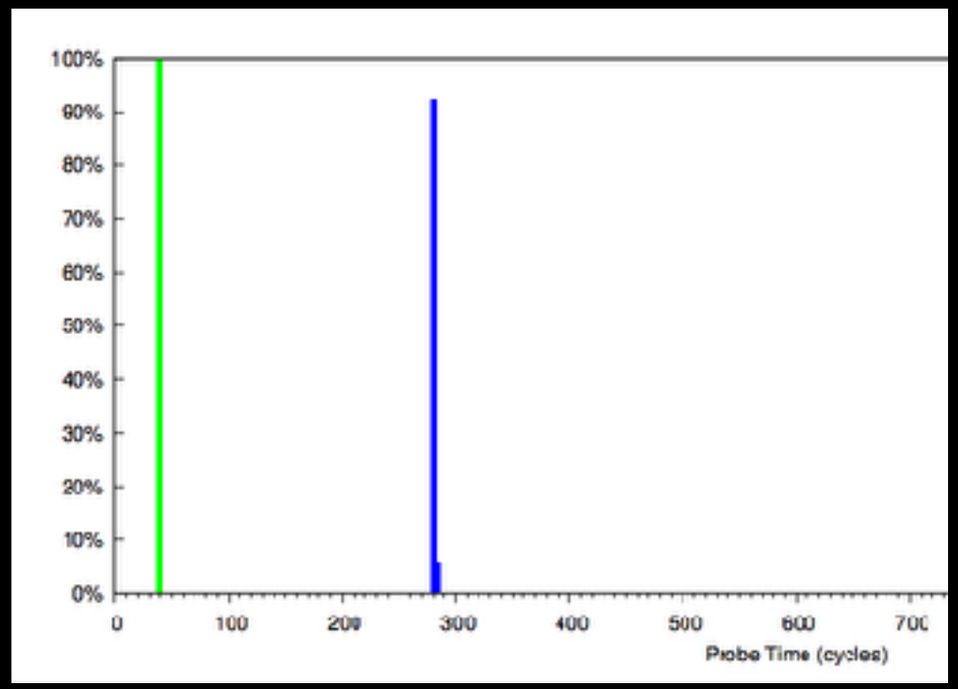

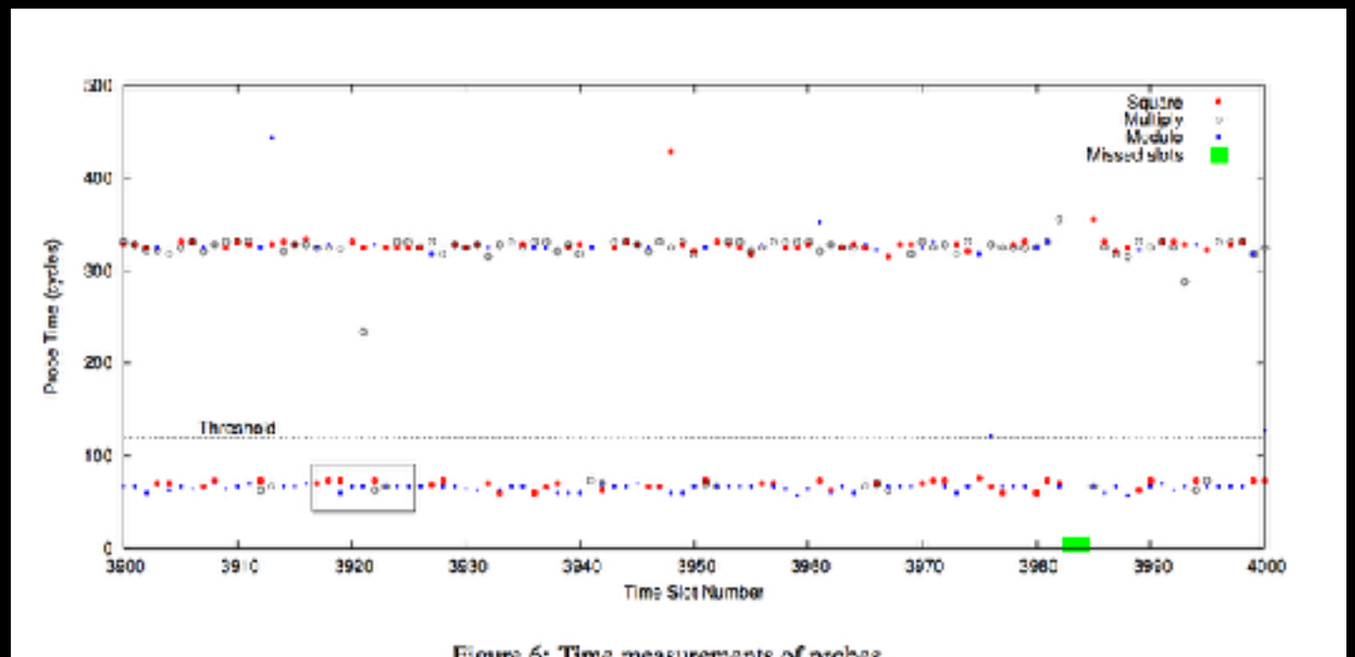

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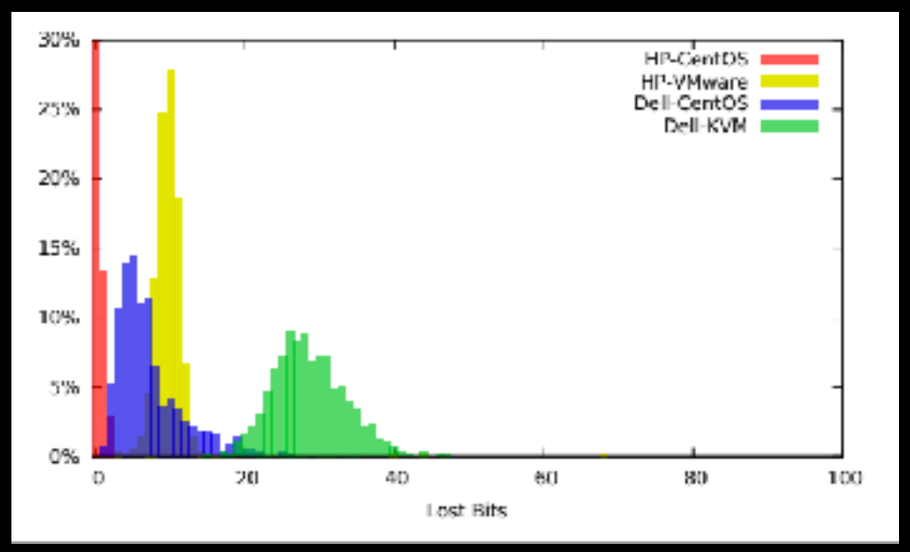

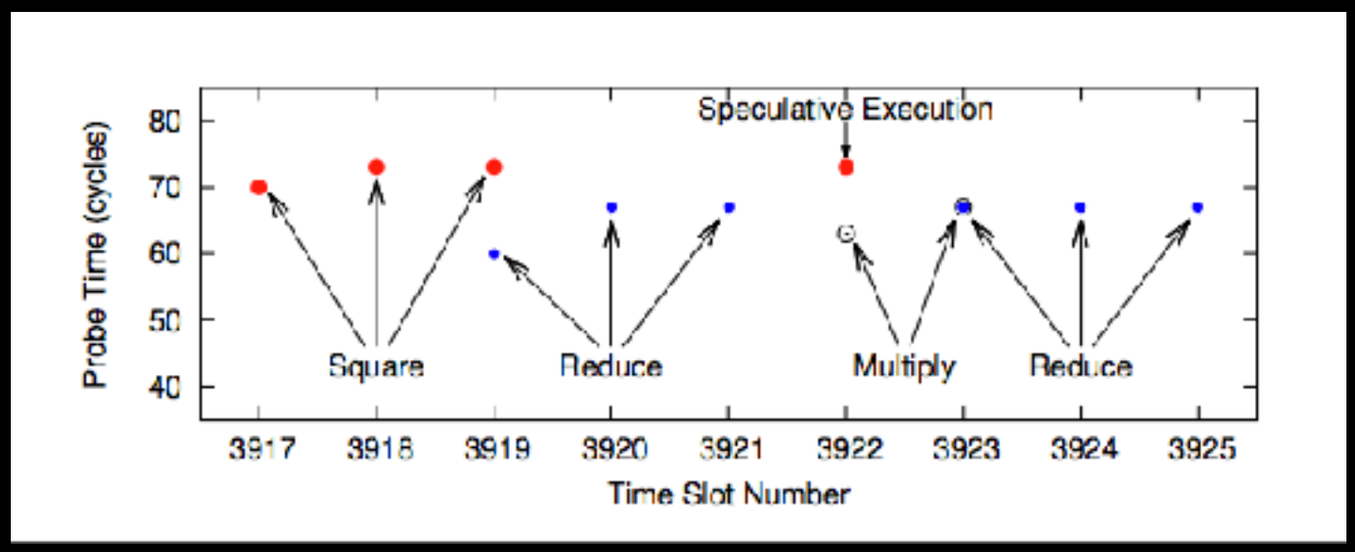

EXAMPLE: FLUSH+RELOAD

- Can also attack AES implementation with T tables
- A table lookup happens $T_j\,[x_i = p_i \oplus k_i\,]$
- p_i is a plaintext byte, k_i a key byte

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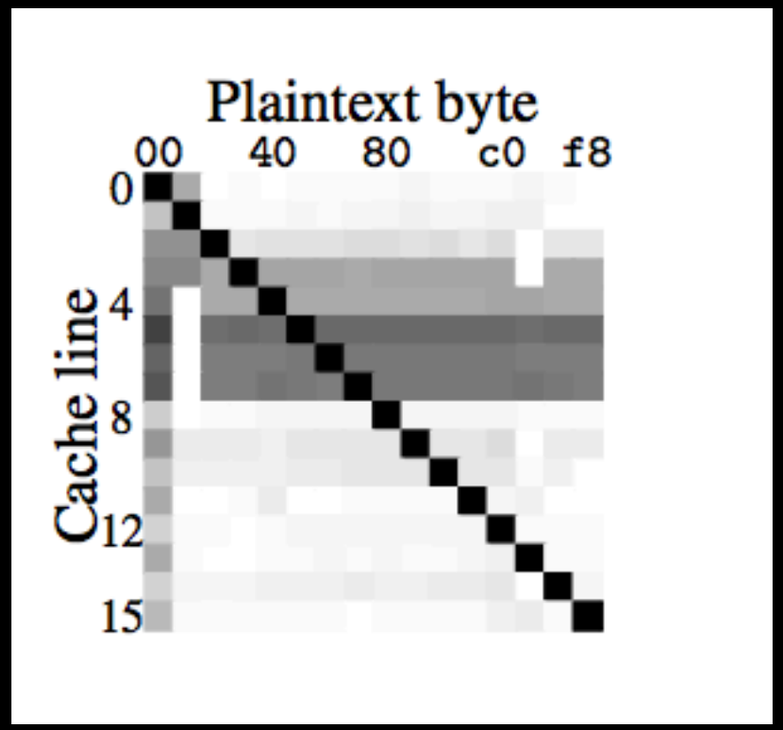

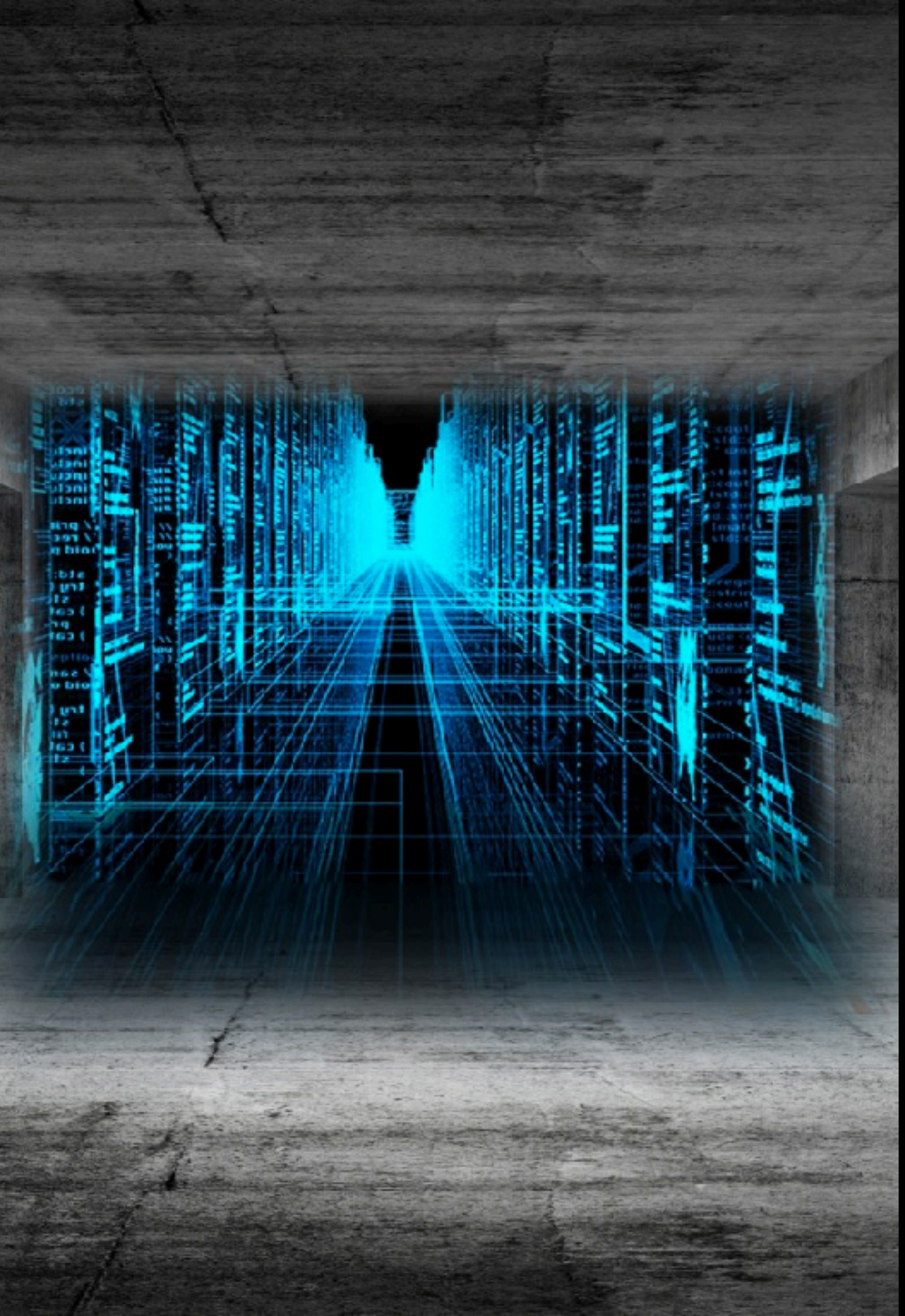

CACHE DEFENCES

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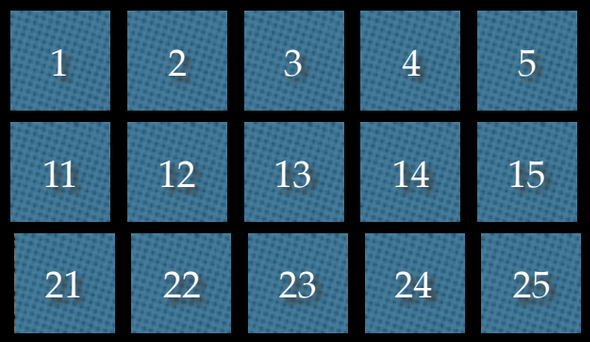

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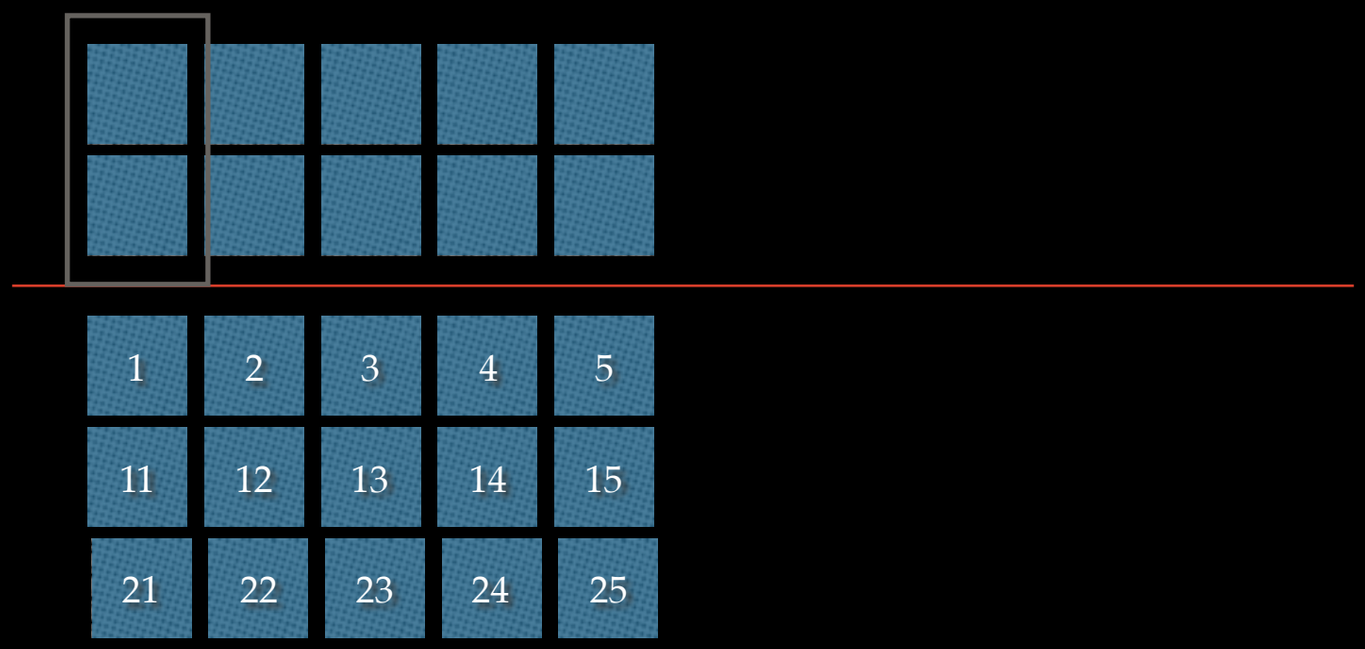

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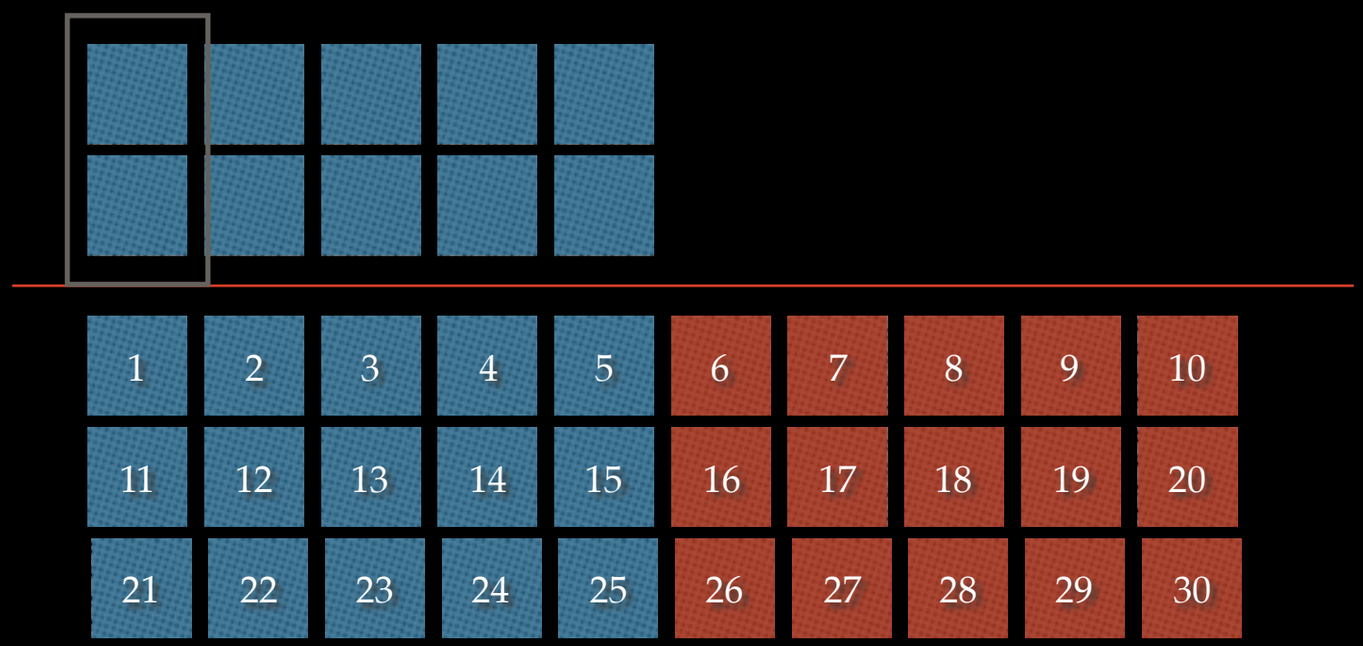

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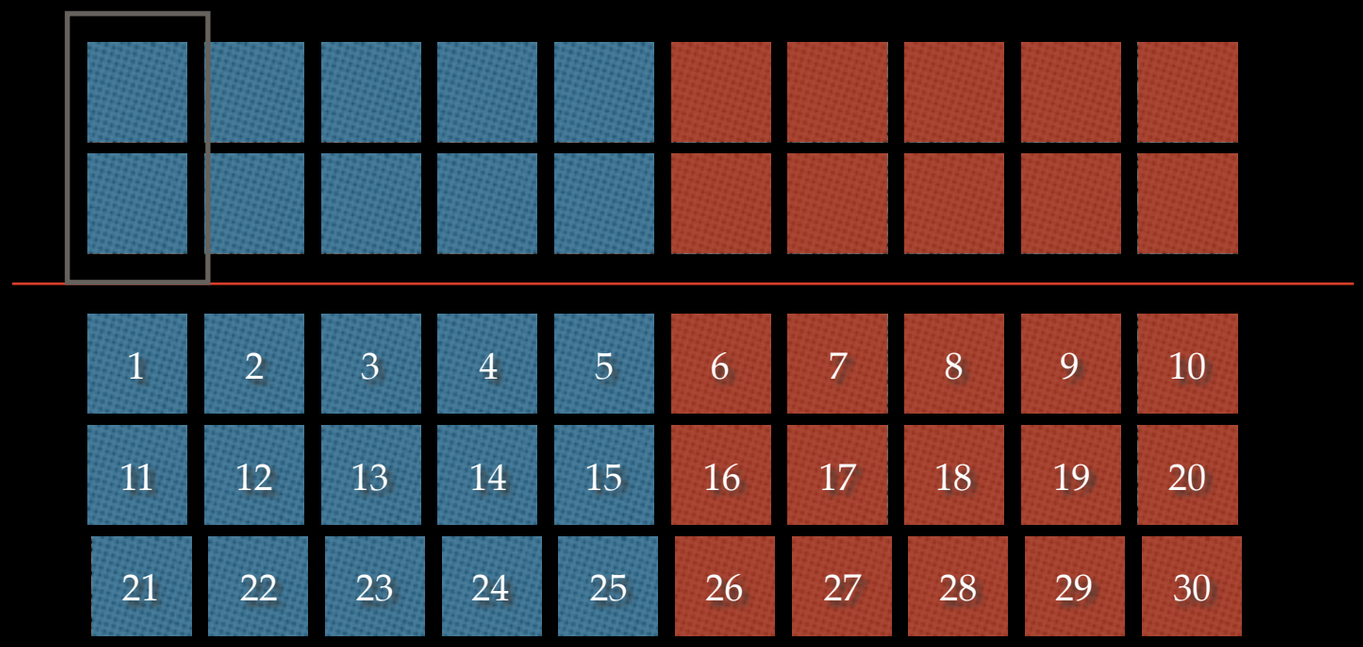

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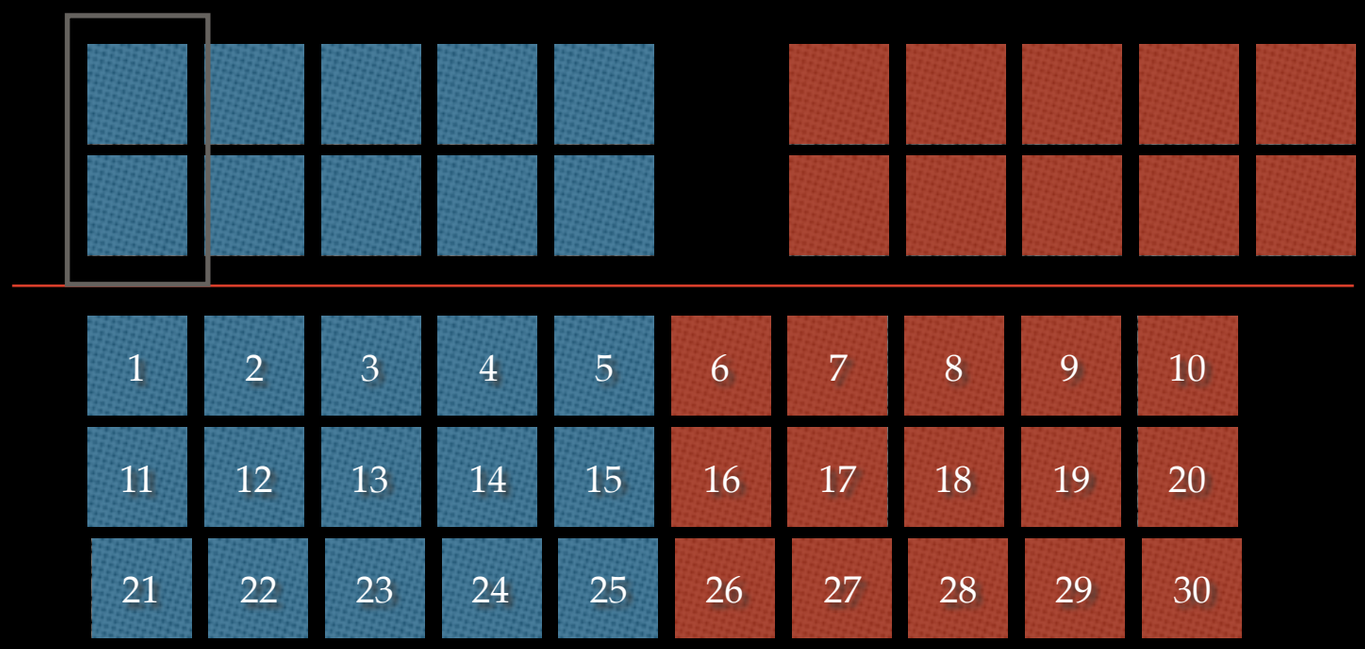

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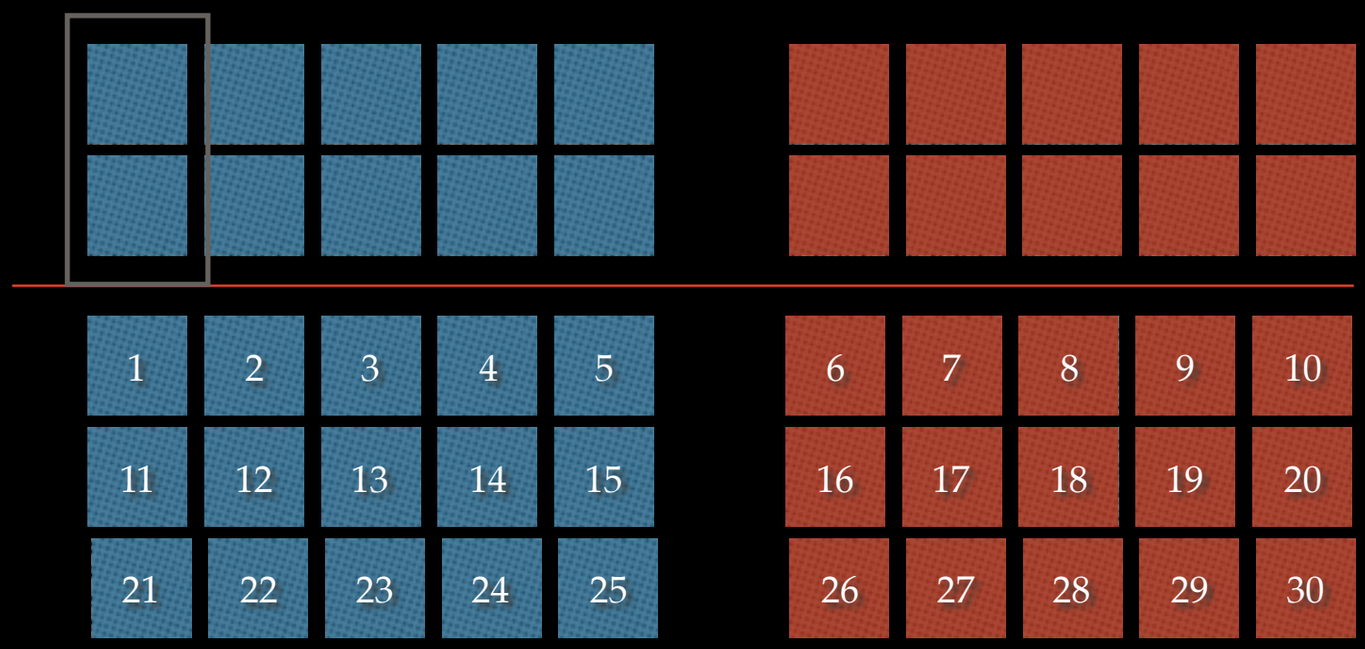

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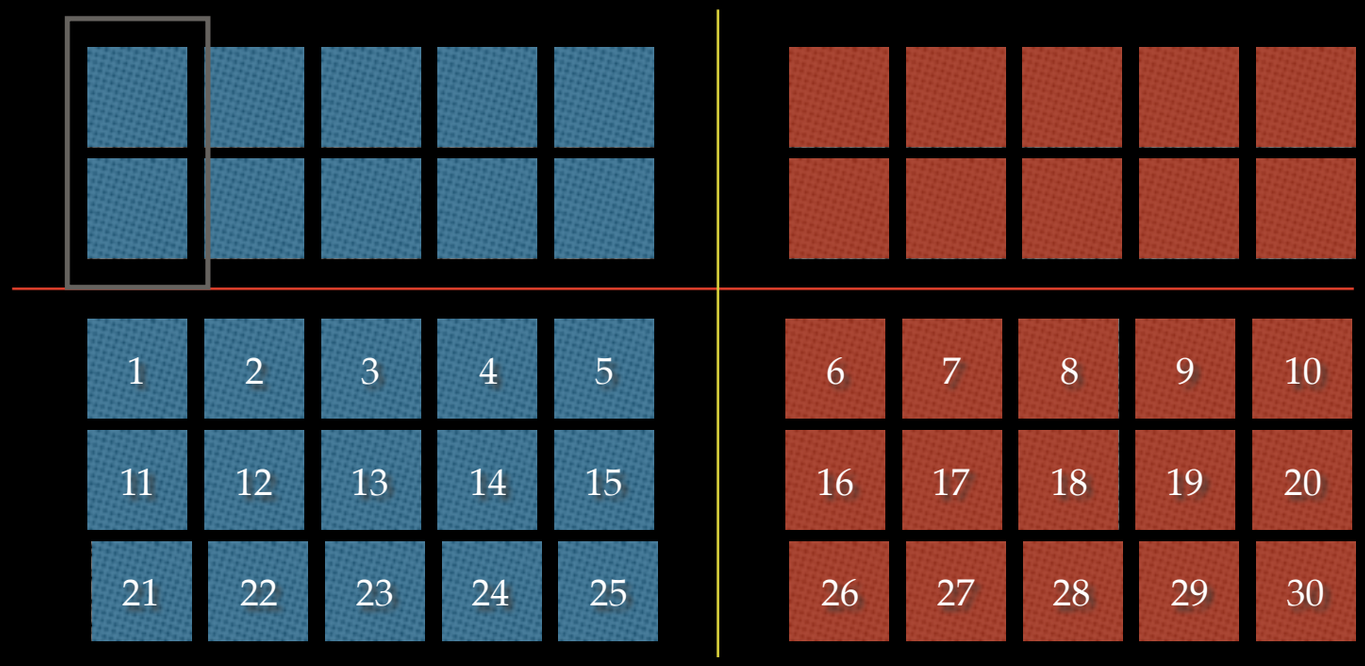

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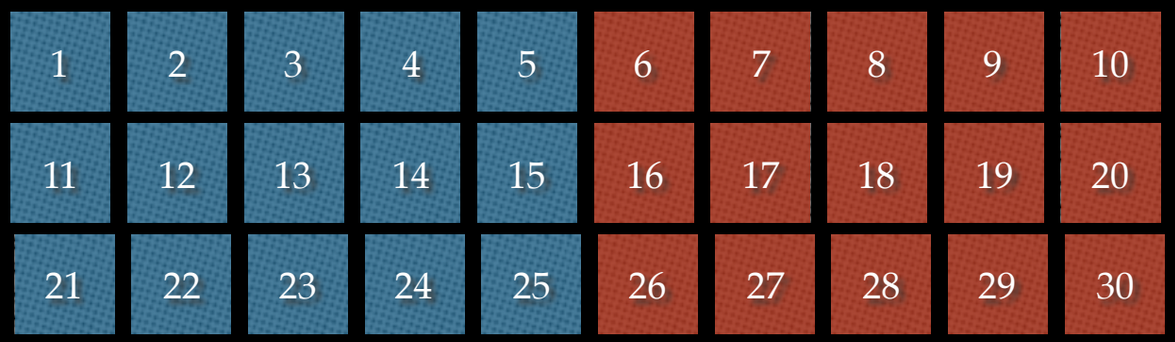

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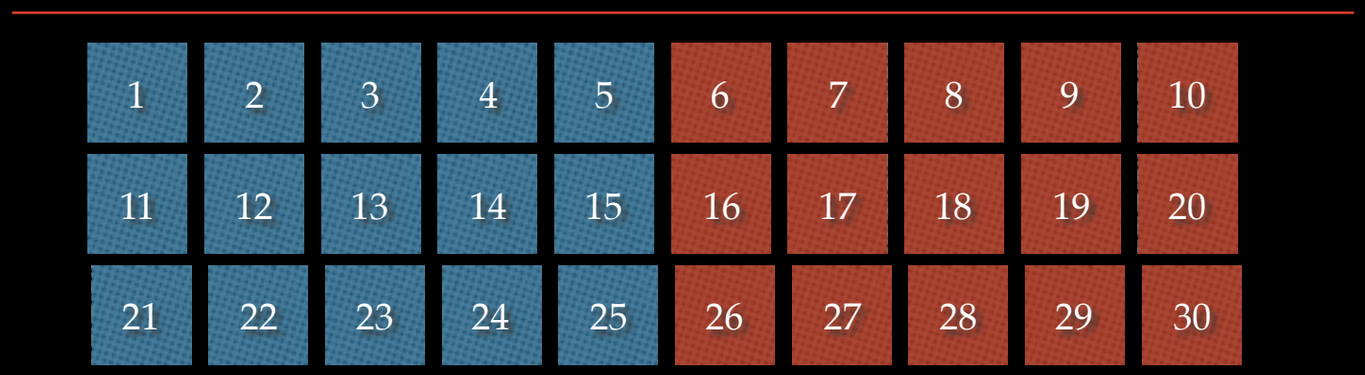

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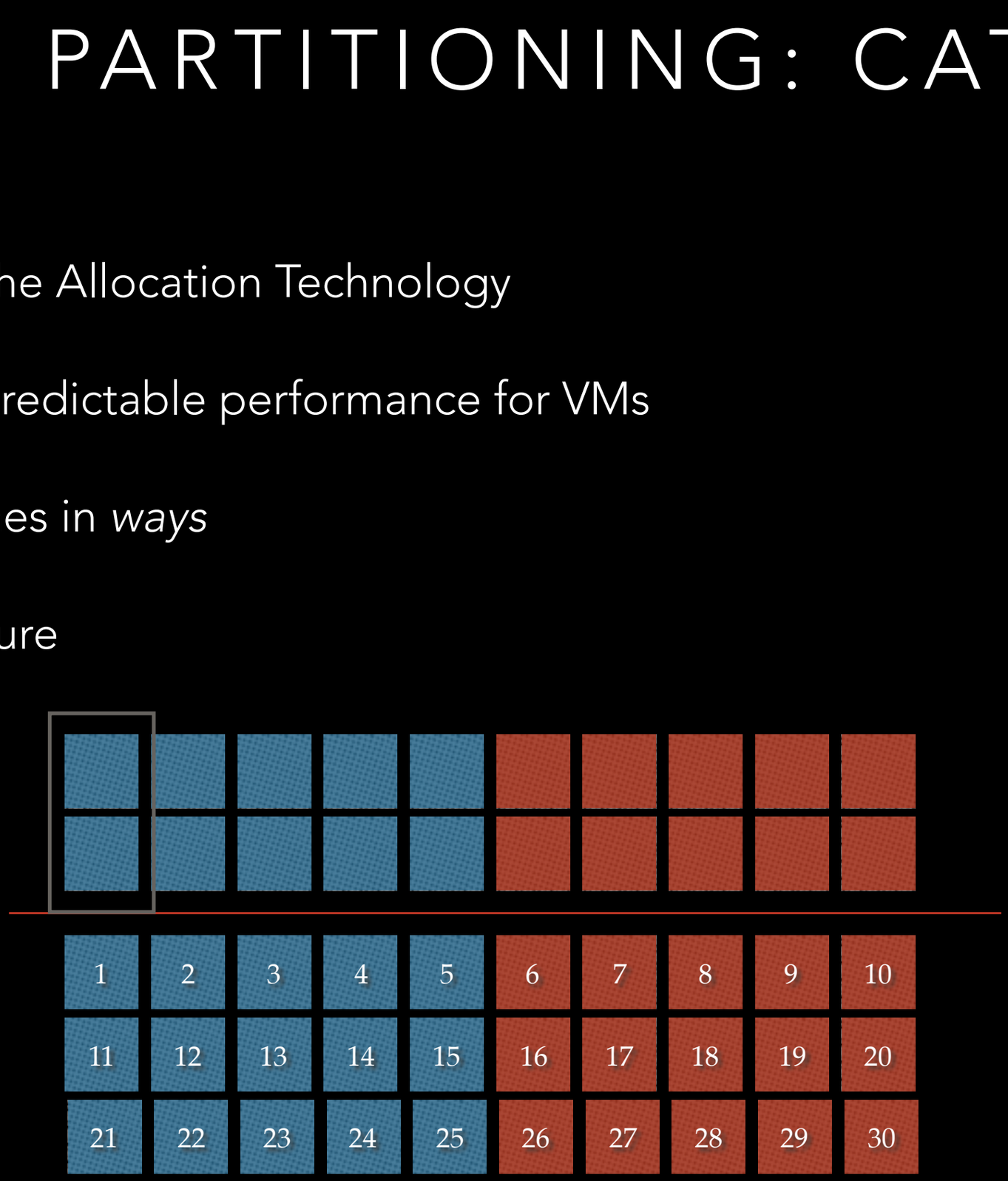

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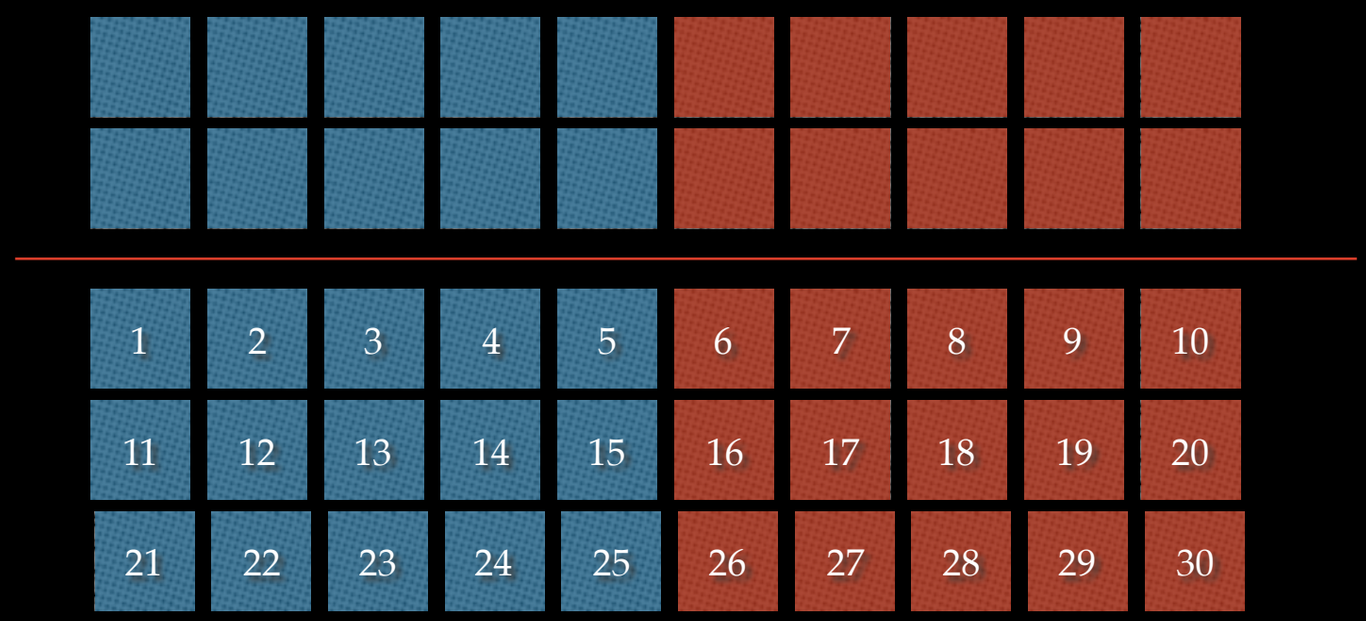

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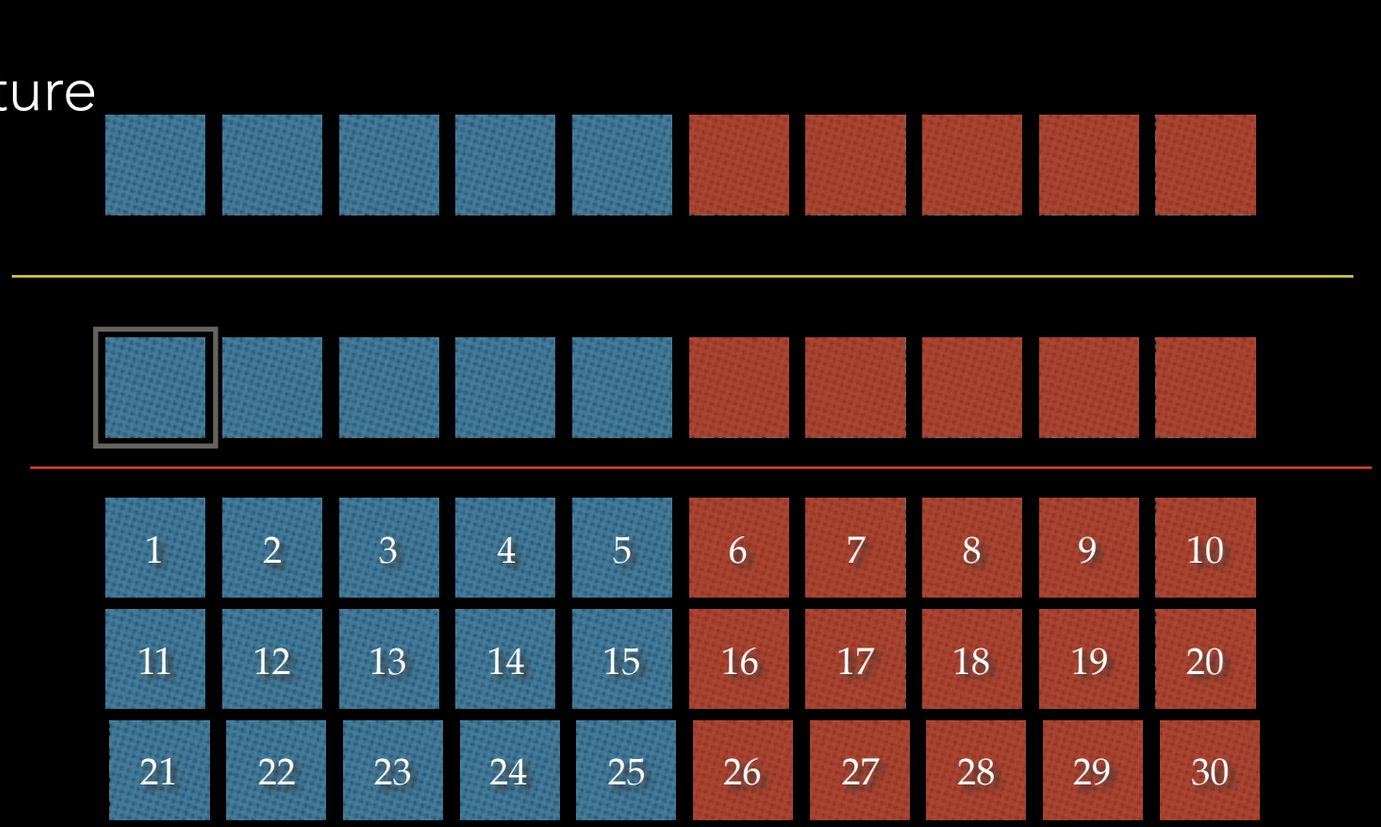

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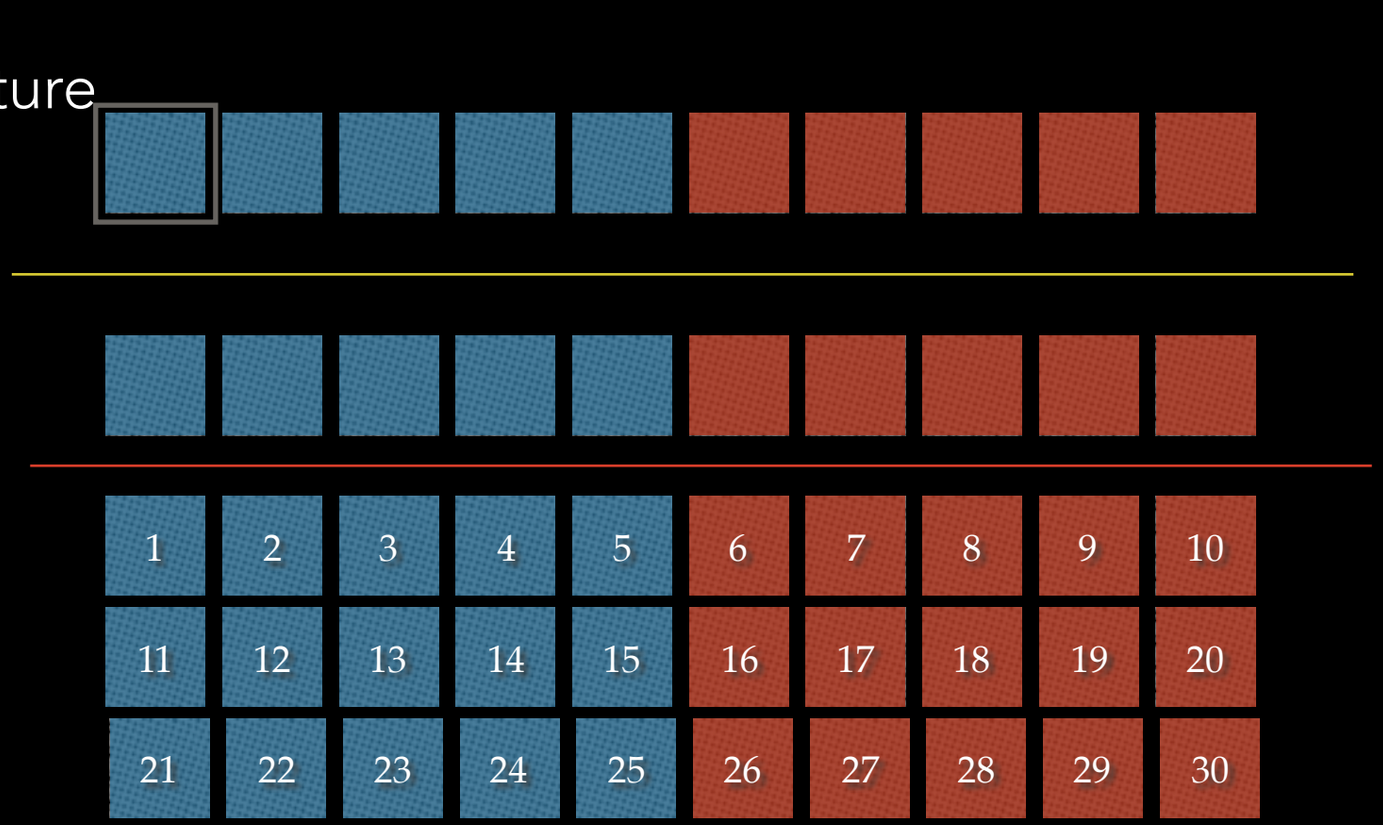

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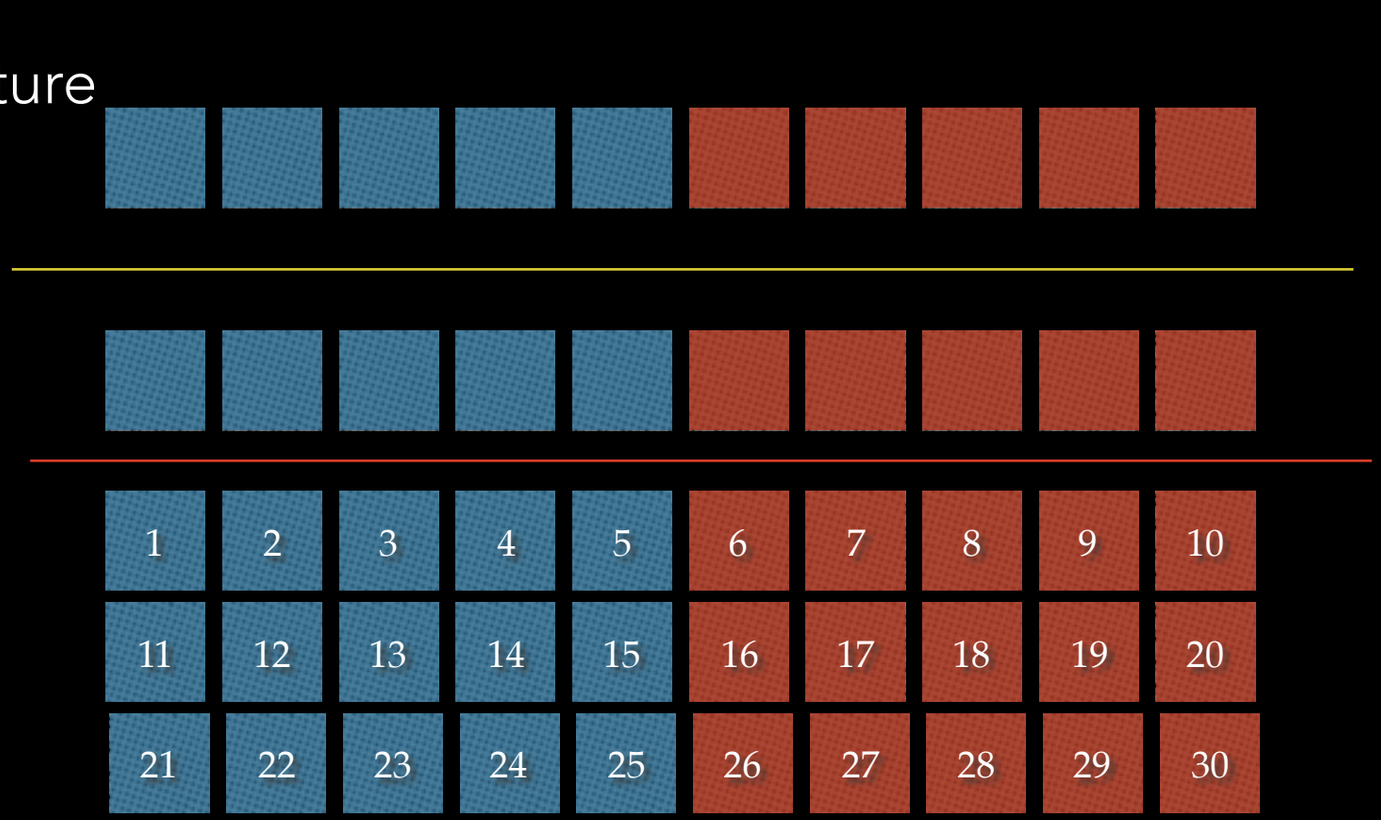

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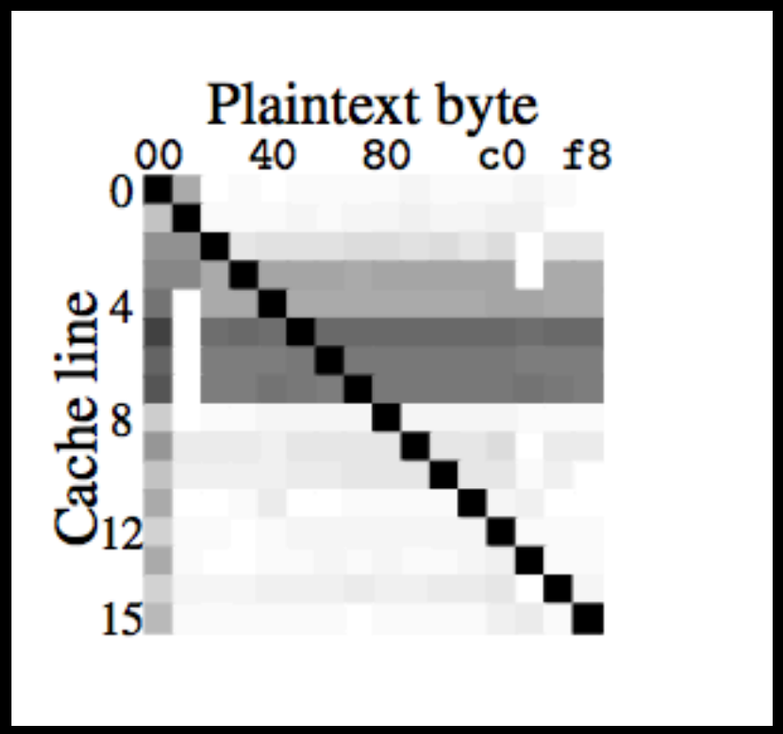

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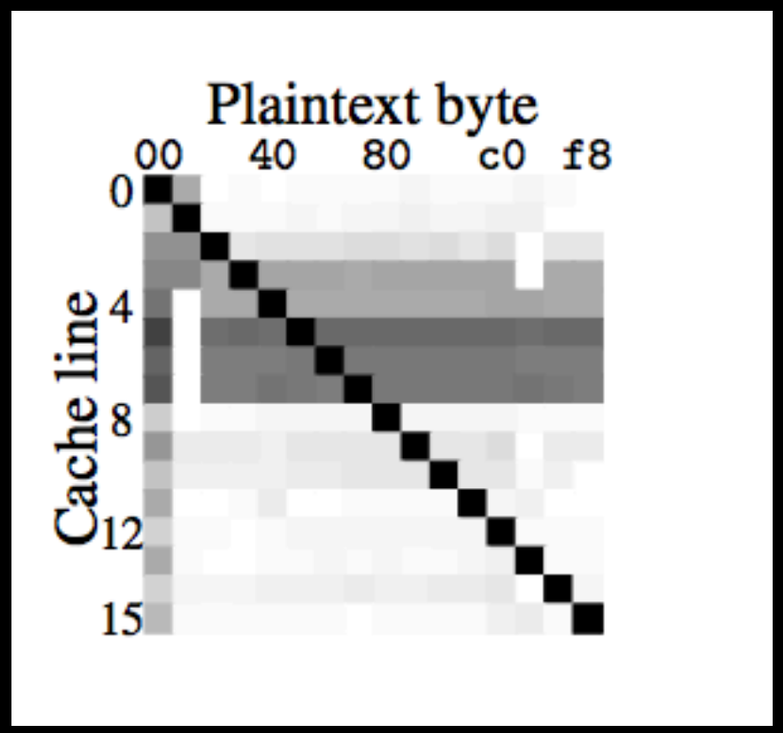
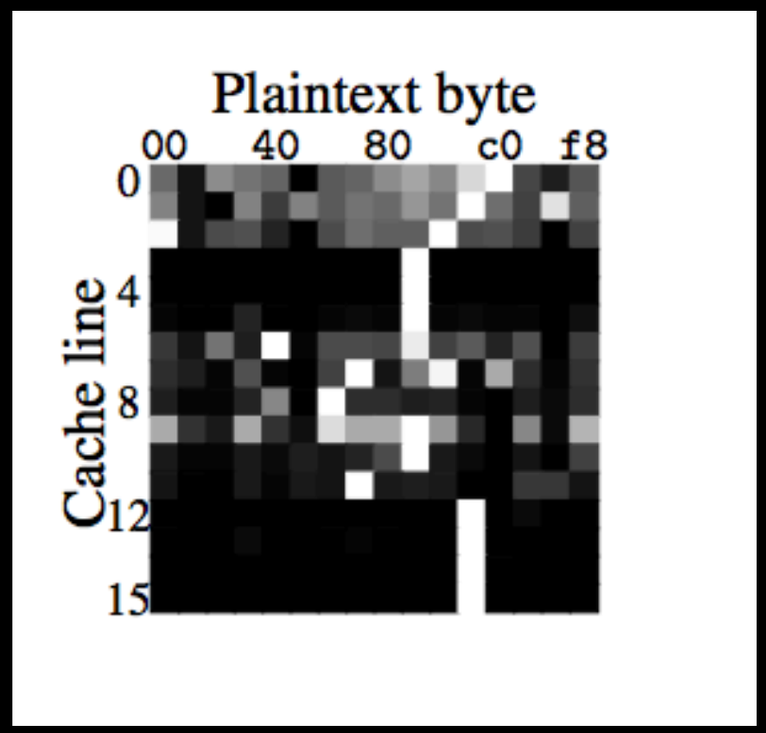
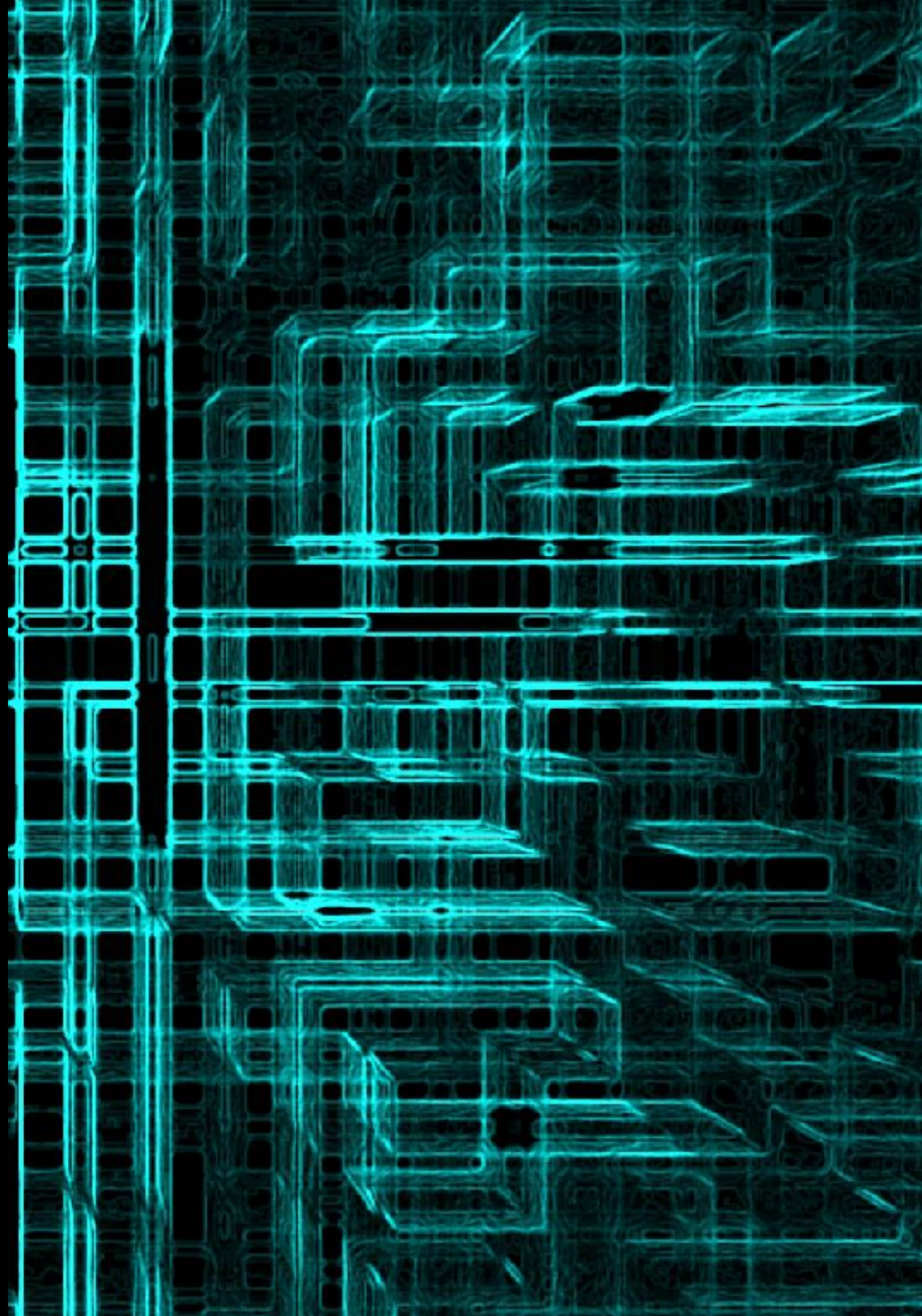




HYPER THREADING



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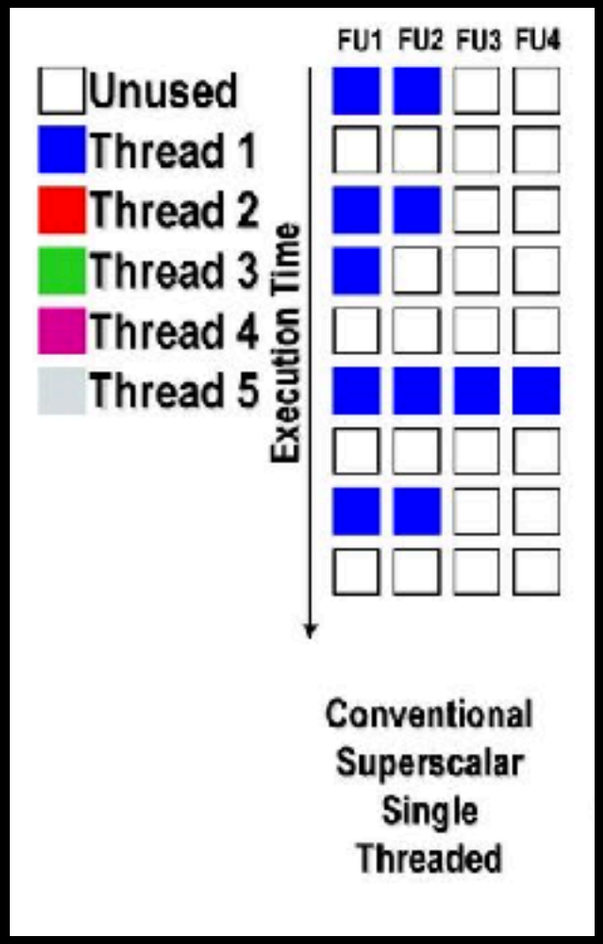

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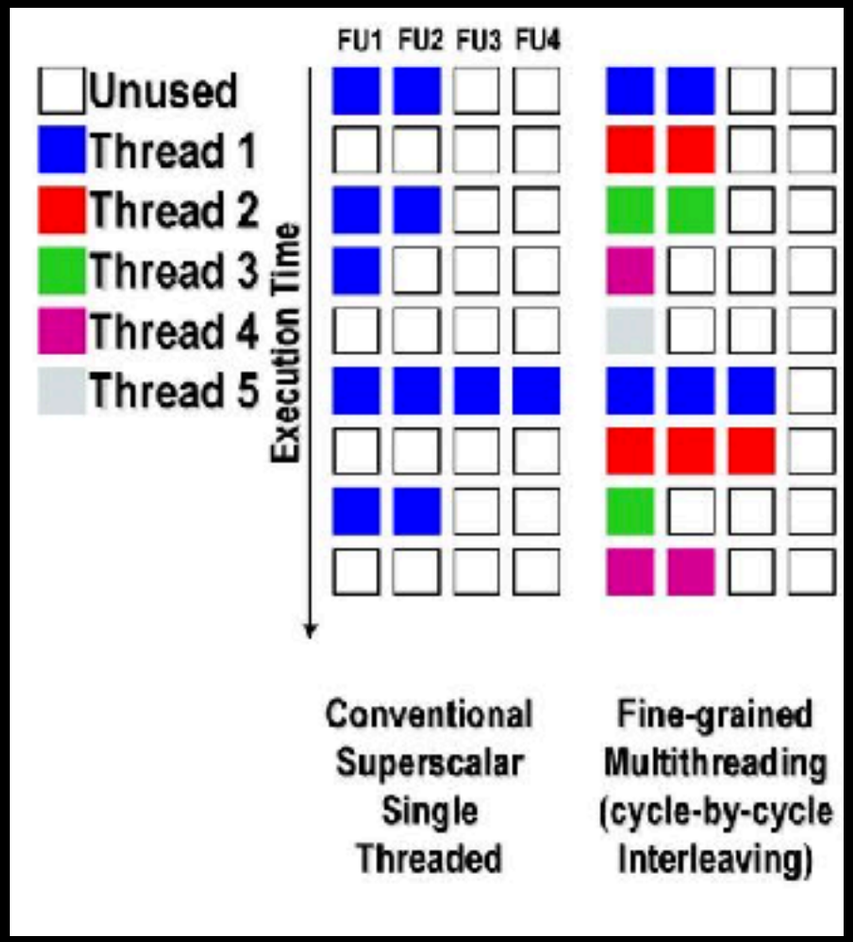

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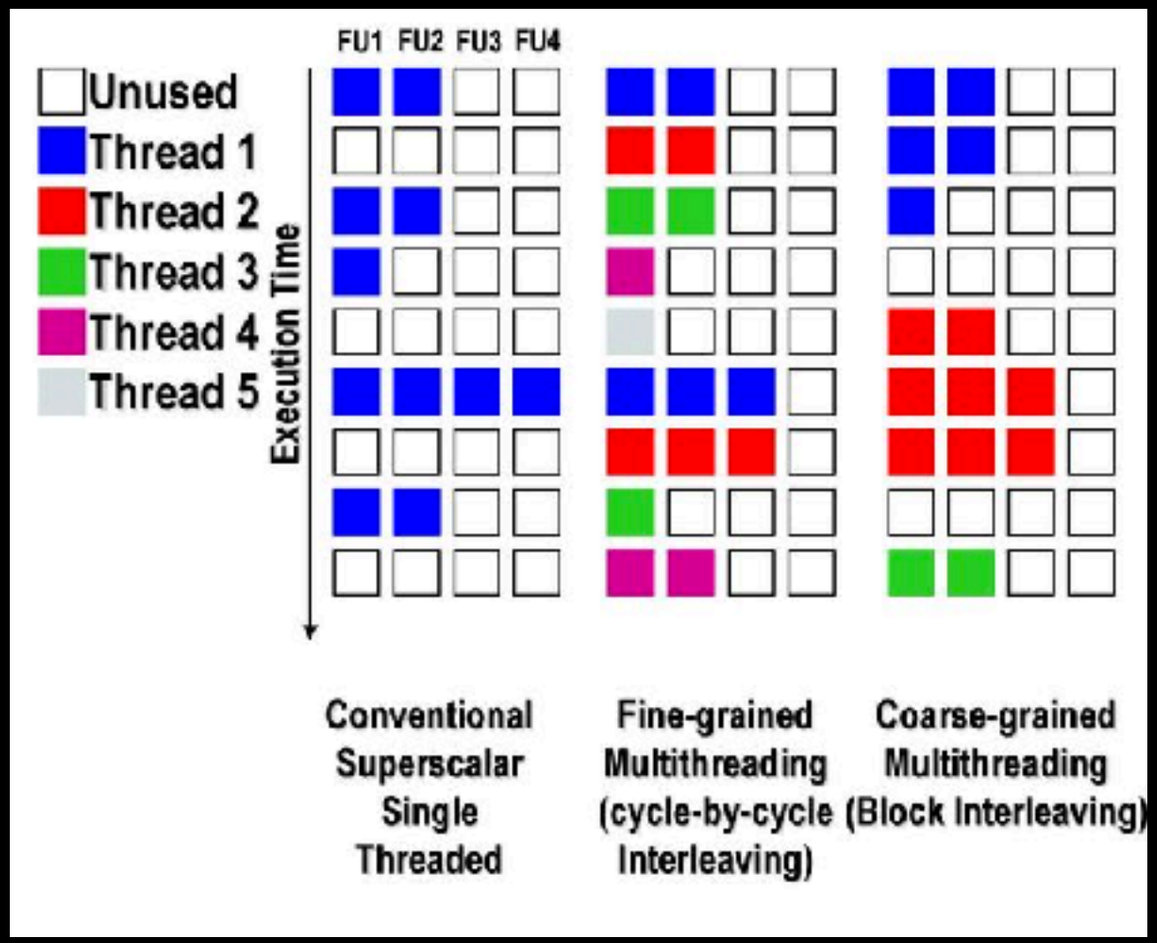

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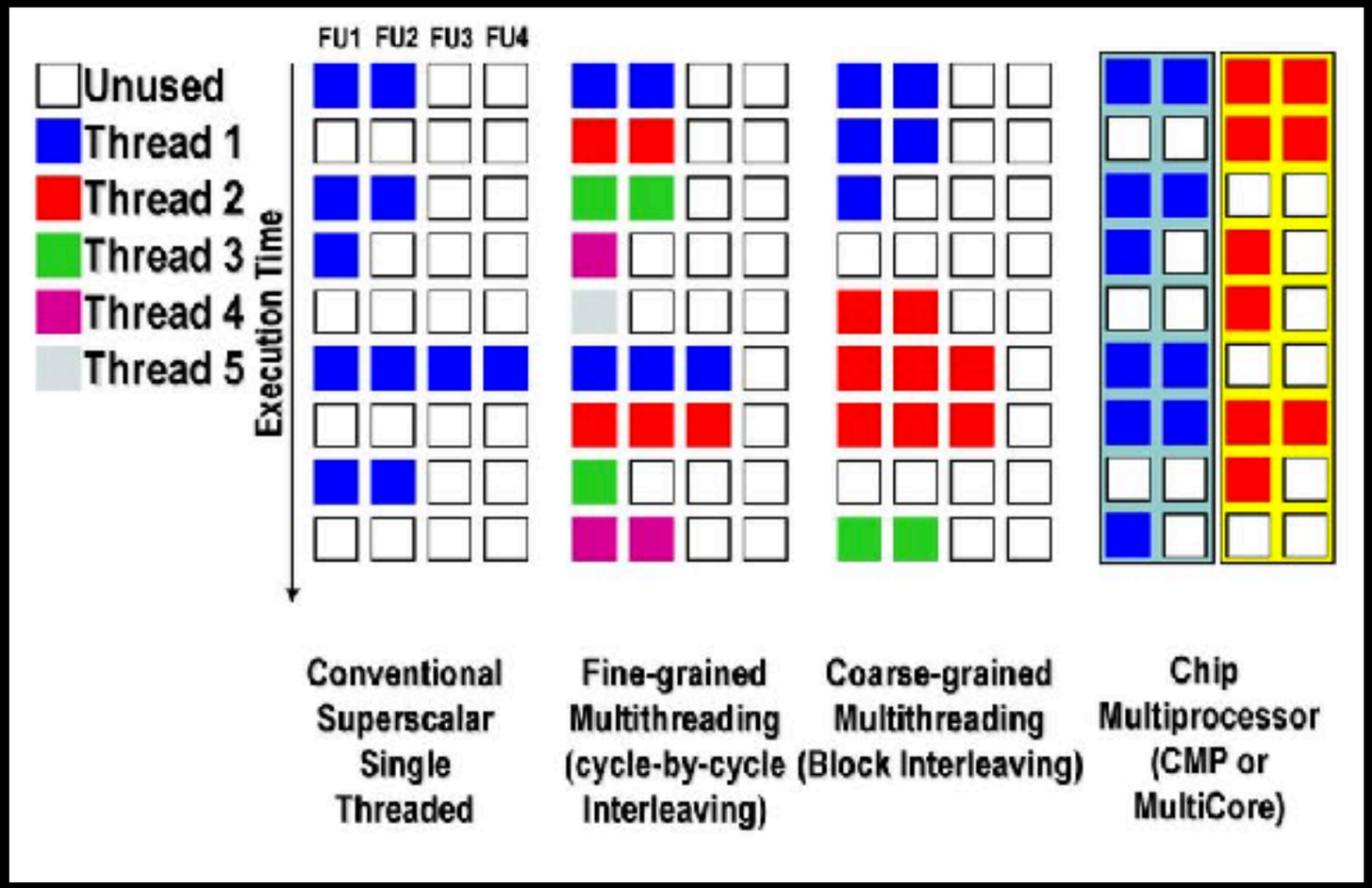

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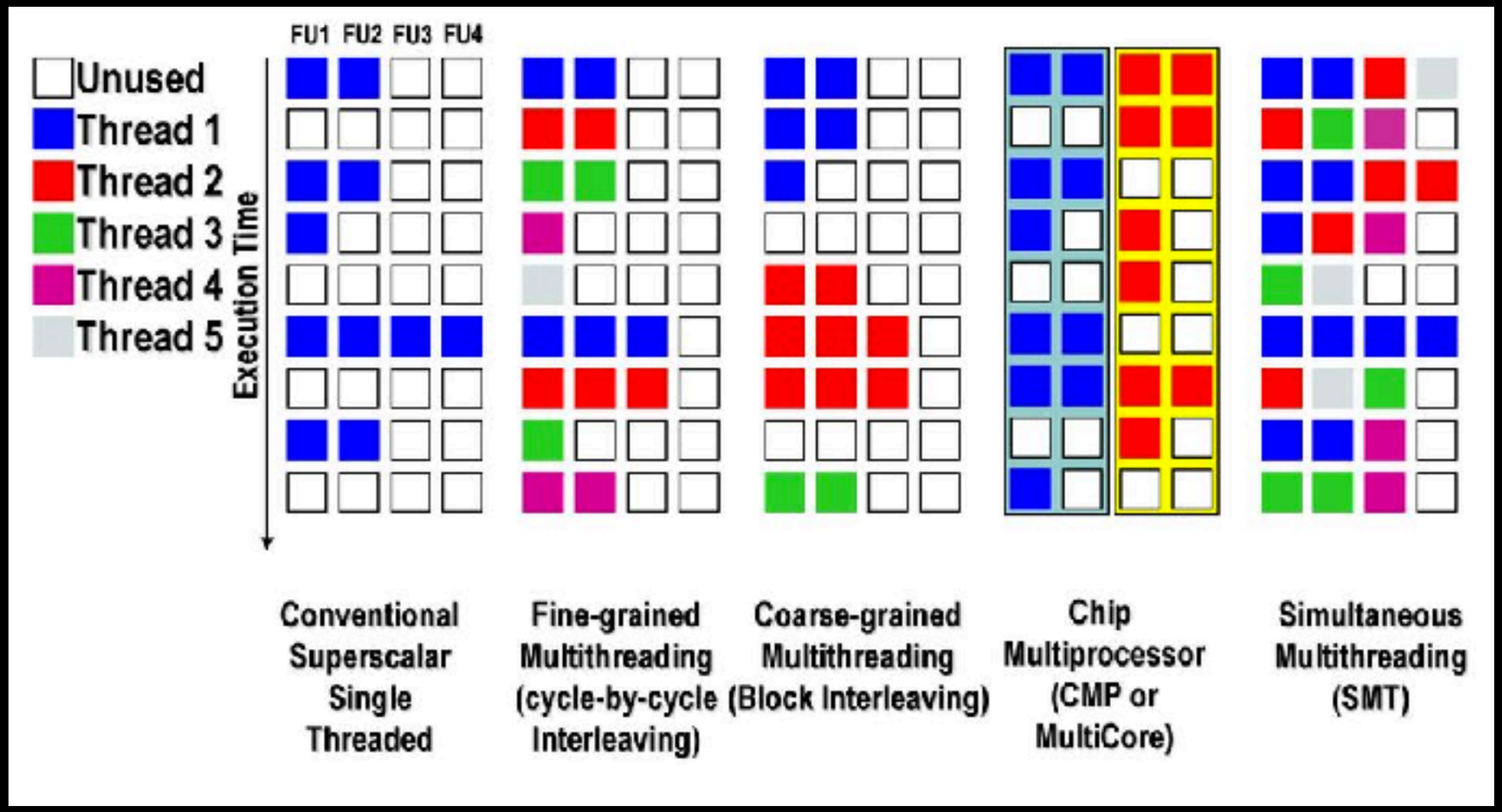

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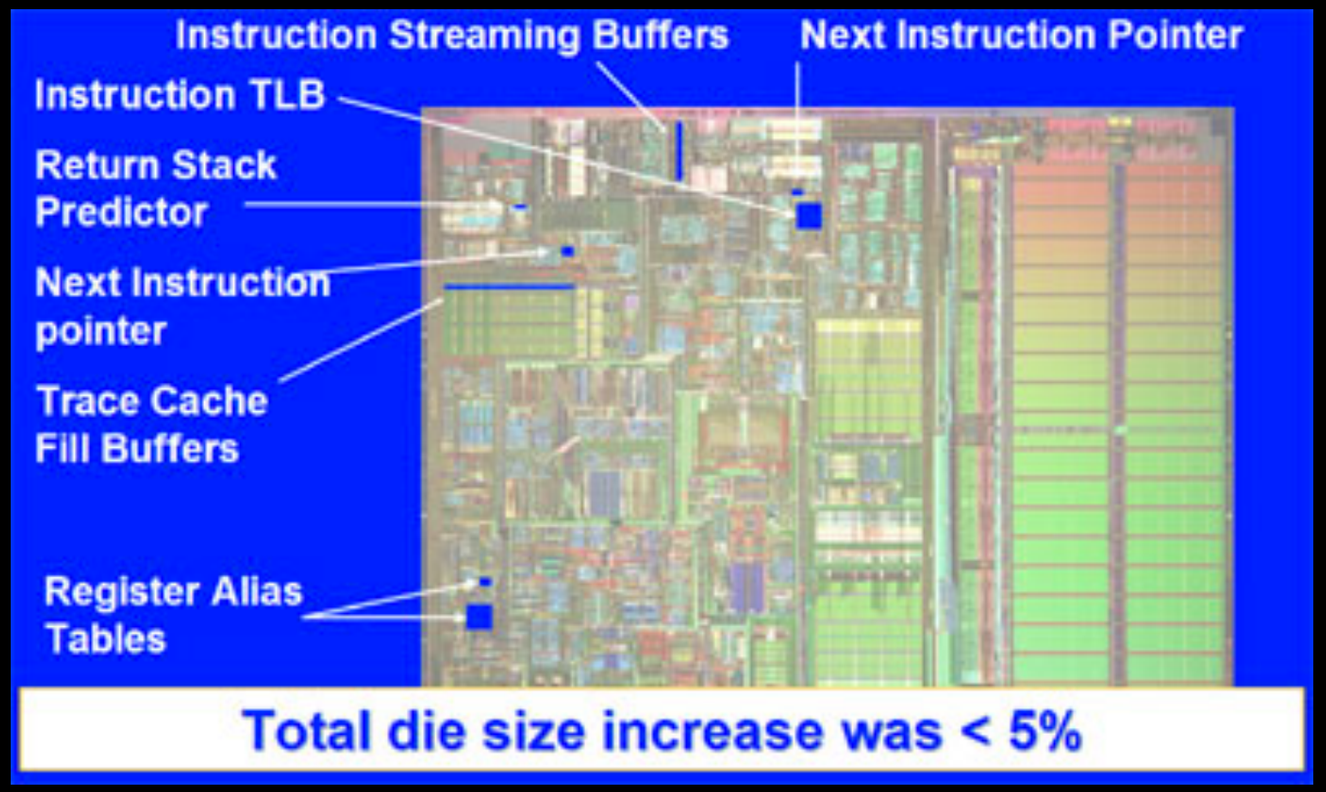

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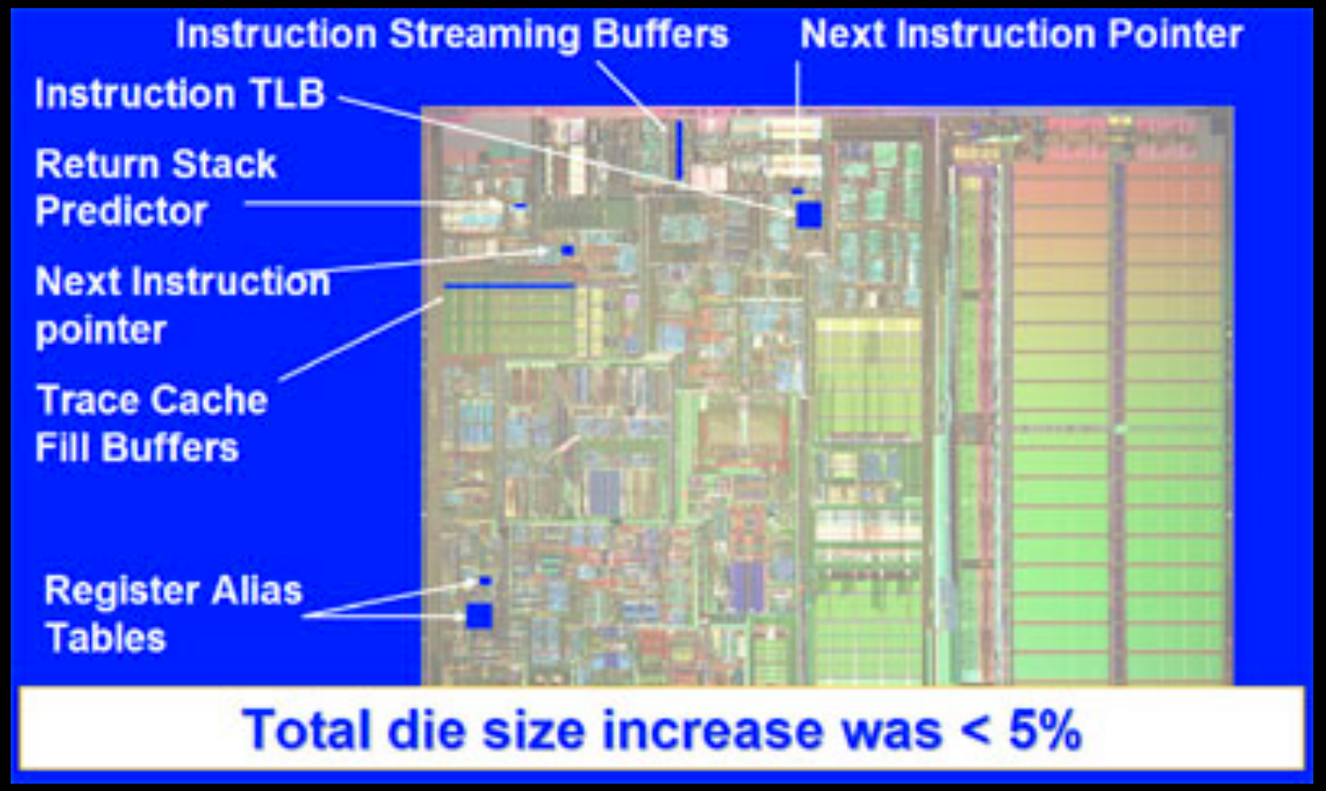
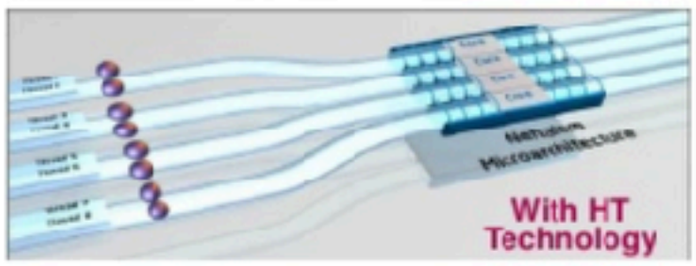


HYPER THREADING

Intel® Hyper-Threading Technology

- Nehalem is a scalable multi-core architecture
- Hyper-Threading Technology augments benefits
  - Power-efficient way to boost performance in all form factors: higher multi-threaded performance, faster multi-tasking response



	Hyper-Threading		Multi-cores
	Shared or Partitioned	Replicated	Replicated
Register State		X	X
Return Stack		X	X
Reorder Buffer	X		X
Instruction TLB	X		X
Reservation Stations	X		X
Cache (L1, L2)	X		X
Data TLB	X		X
Execution Units	X		X

- Next generation Hyper-Threading Technology:
  - Low-latency pipeline architecture
  - Enhanced cache architecture
  - Higher memory bandwidth

HYPER THREADING

- Significant resource sharing: good and bad

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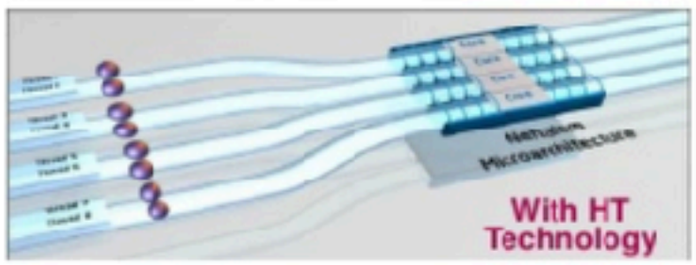

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TLBLEED

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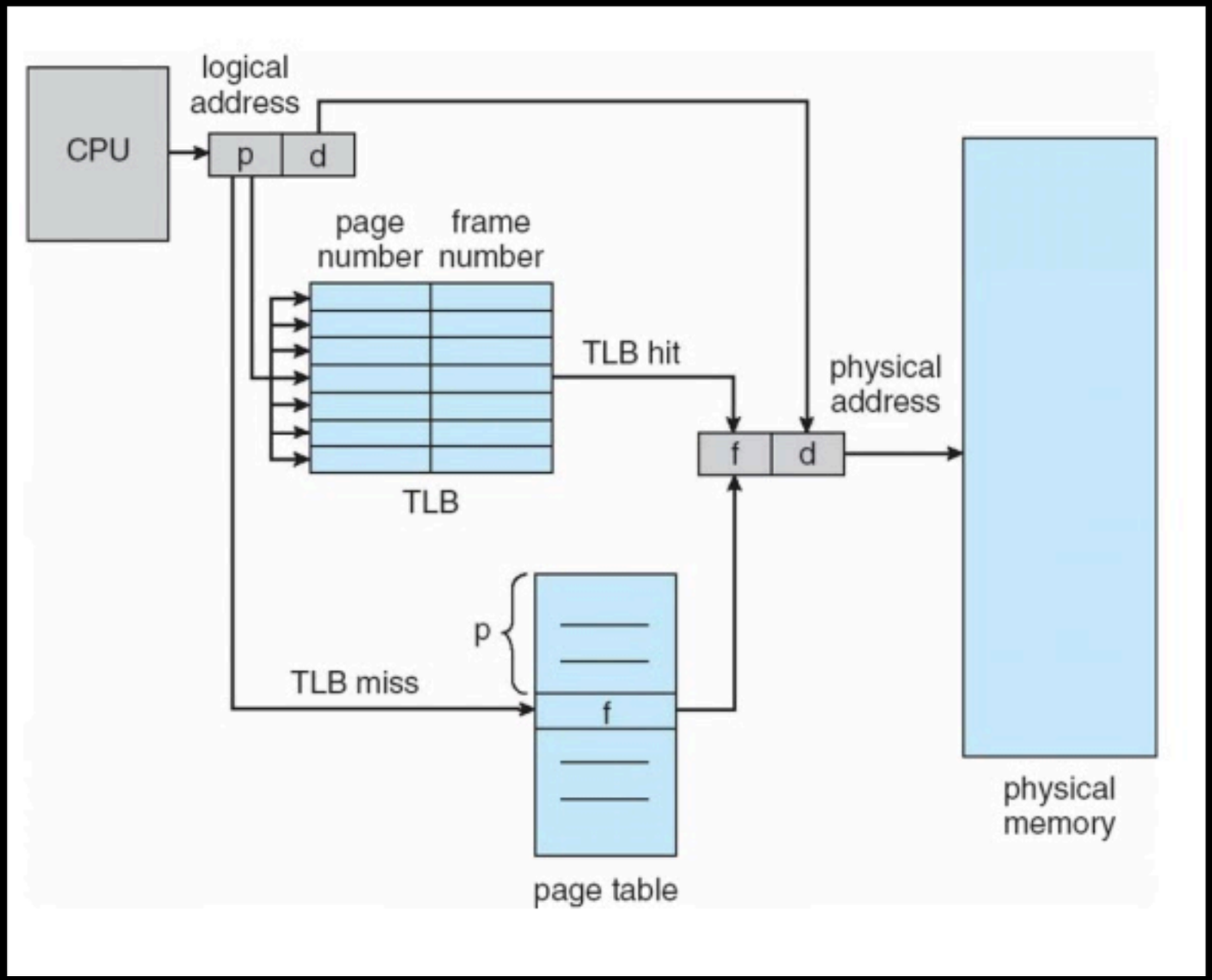
CPU
logical address
p
d
page number
frame number
TLB hit
physical address
f
d
TLB
p
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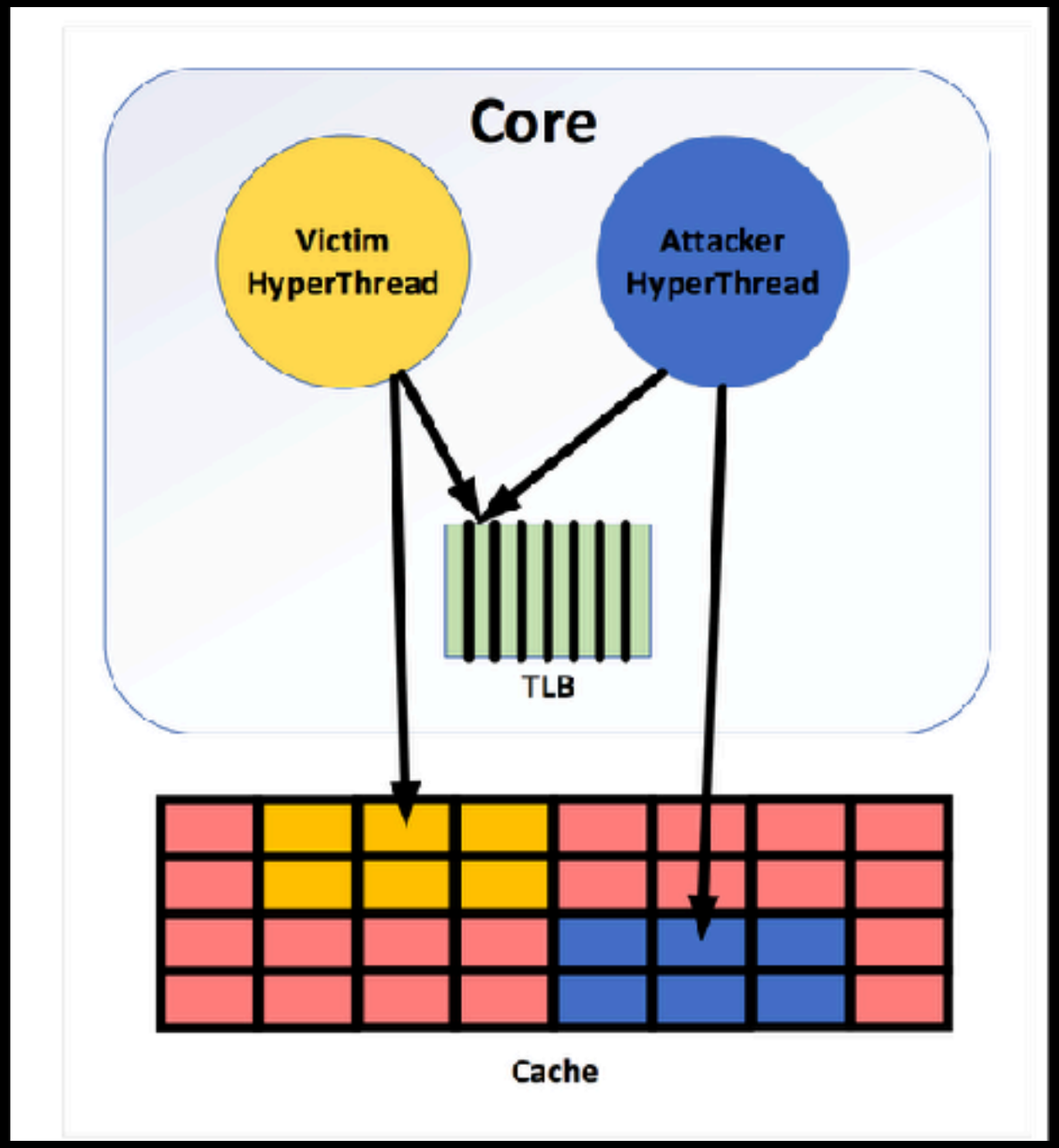
f
page table
physical memory

TLBLEED: TLB AS SHARED STATE



TLBLEED: TLB AS SHARED STATE

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- Other structures than cache shared between threads?
- What about the TLB?
- Documented: TLB has L1iTLB, L1dTLB, and L2TLB
- They have sets and ways
- Not documented: structure

TLBLEED: TLB AS SHARED STATE

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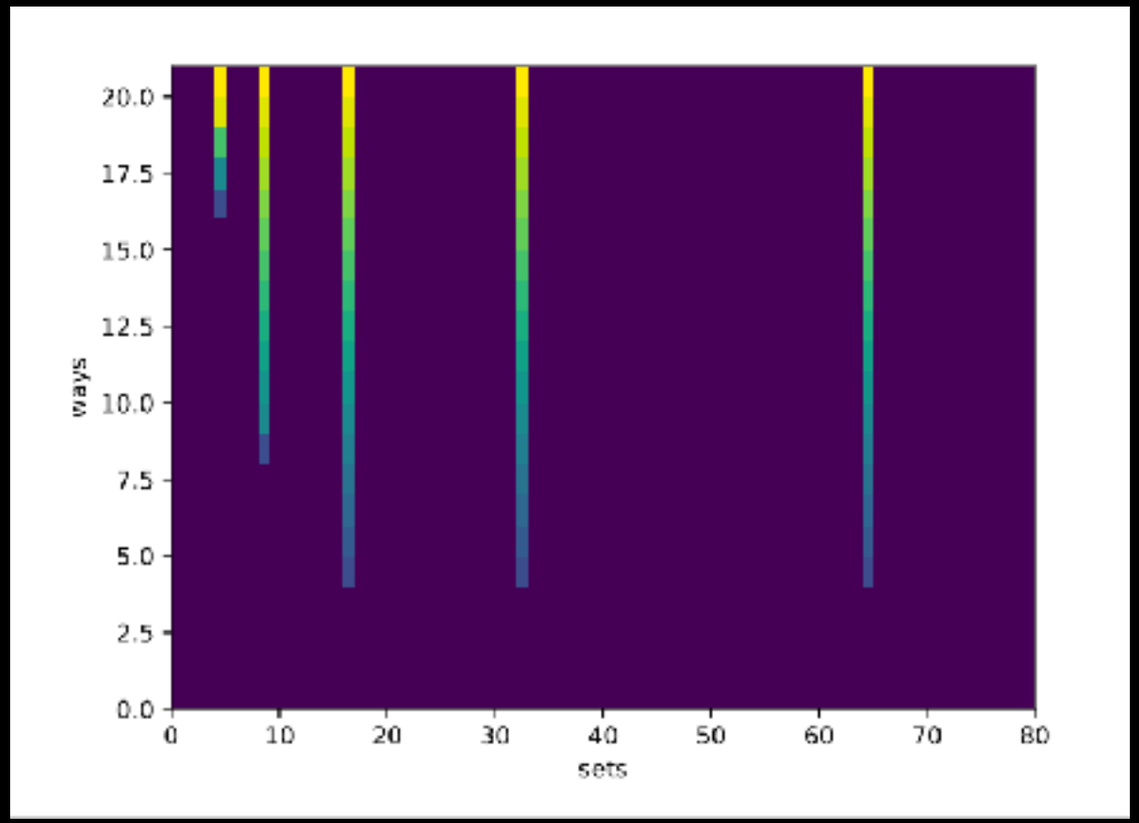

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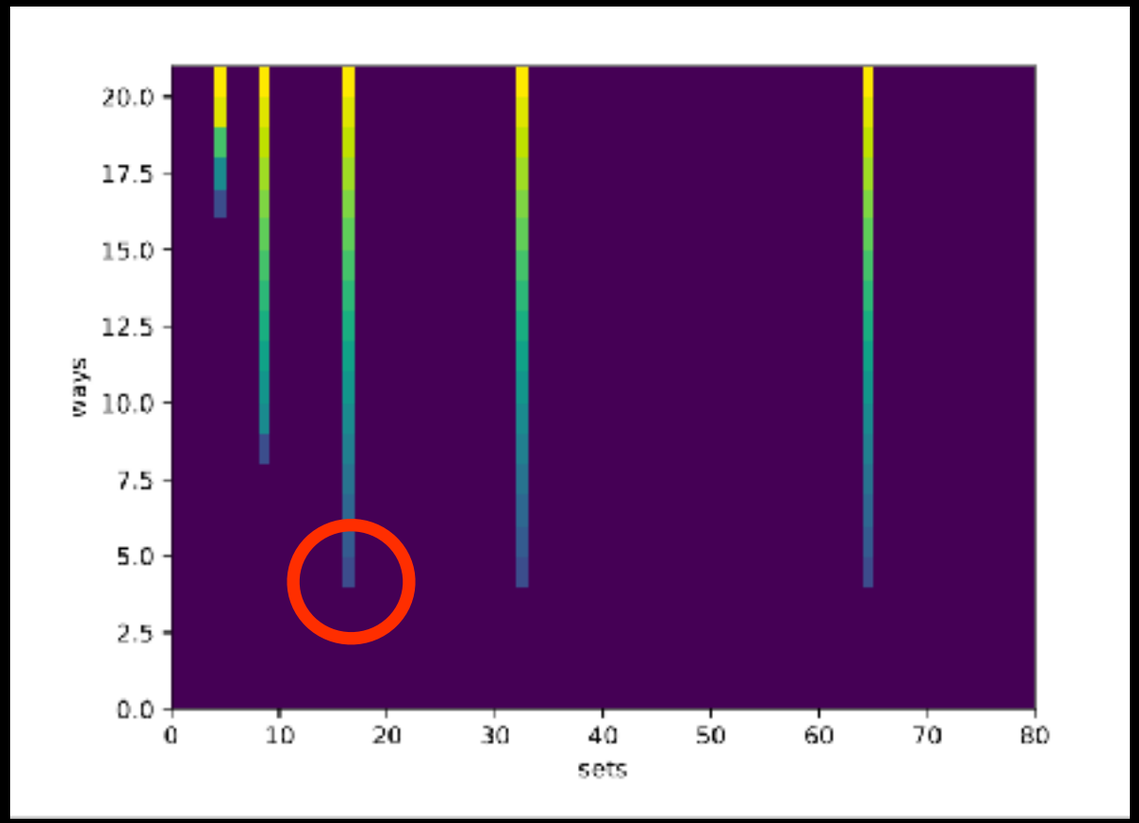

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$$H = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

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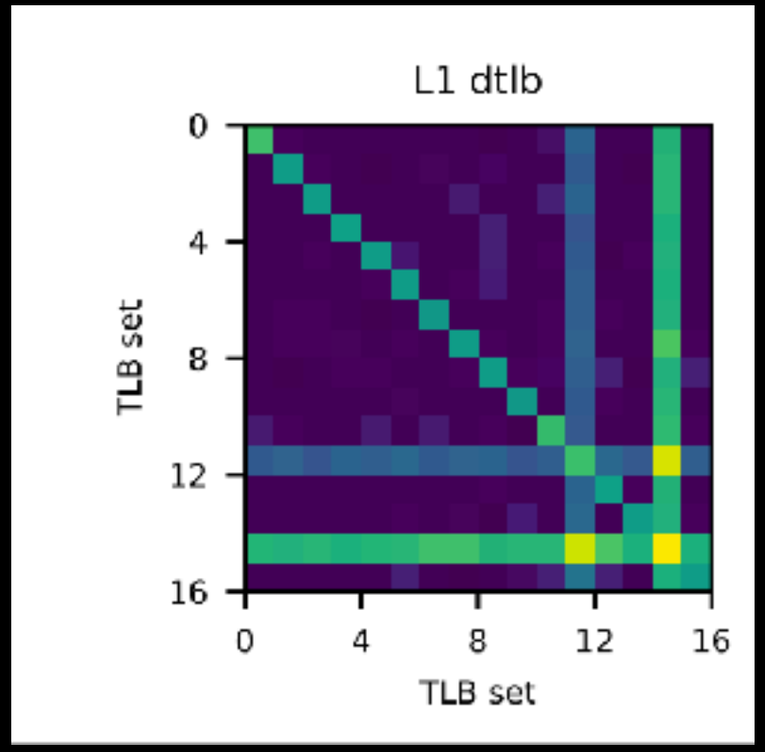

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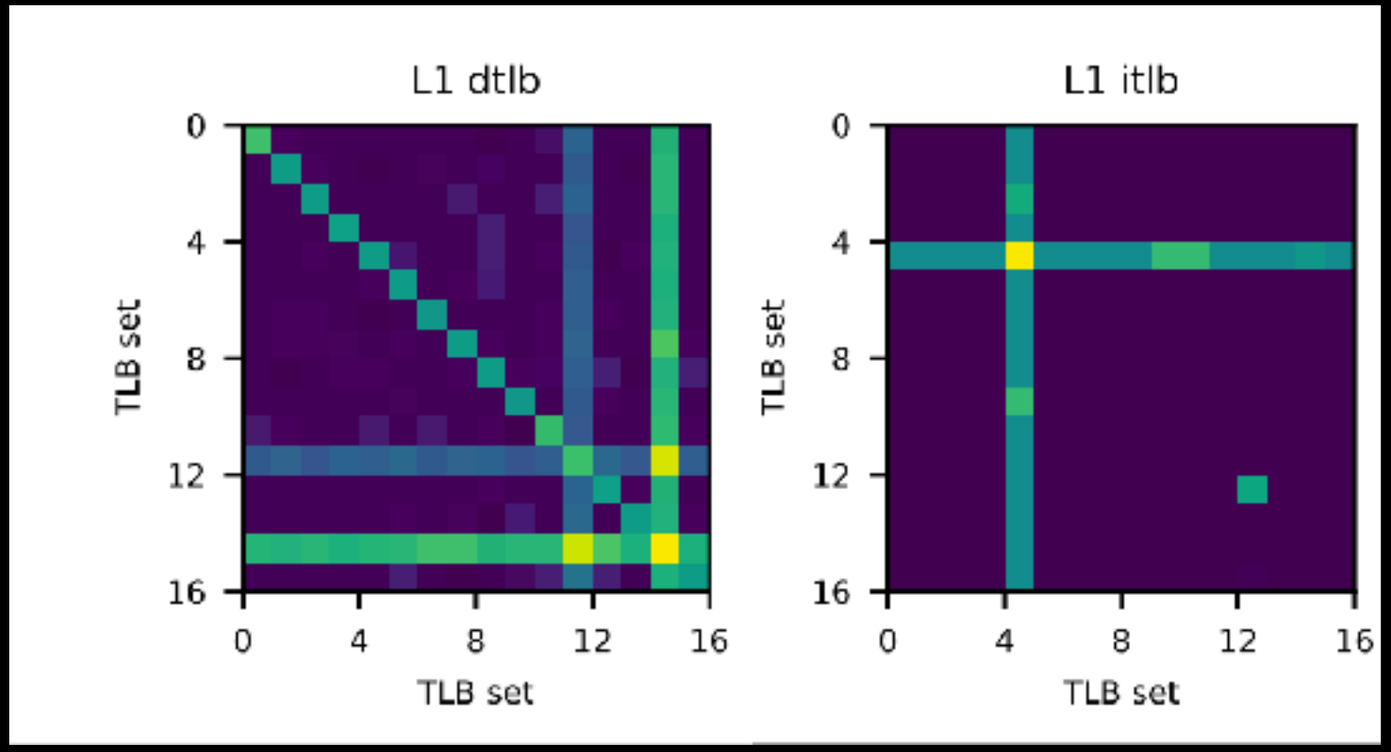

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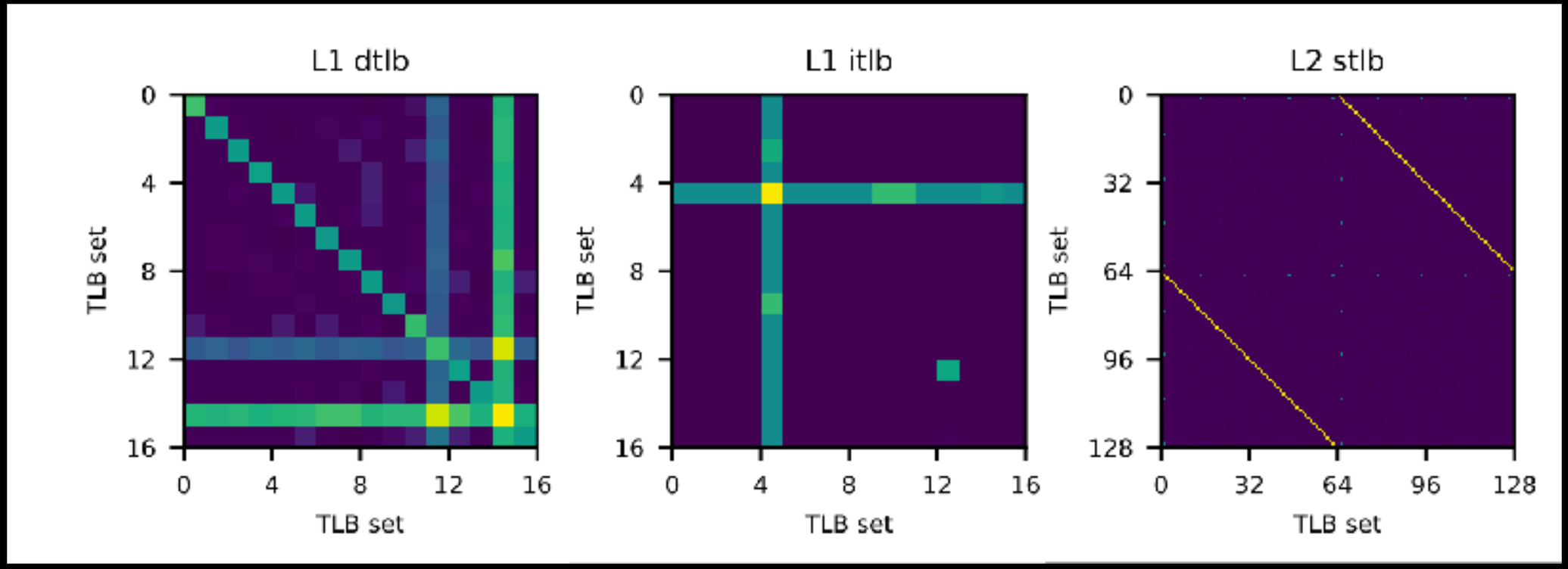

TLBLEED: TLB AS SHARED STATE

		L1 dTLB					L1 iTLB					L2 sTLB				
Name	year	set	w	pn	hsh	shr	set	w	pn	hsh	shr	set	w	pn	hsh	shr
Sandybridge	2011	16	4	7.0	lin	✓	16	4	50.0	lin	✗	128	4	16.3	lin	✓
Ivybridge	2012	16	4	7.1	lin	✓	16	4	49.4	lin	✗	128	4	18.0	lin	✓
Haswell	2013	16	4	8.0	lin	✓	8	8	27.4	lin	✗	128	8	17.1	lin	✓
HaswellXeon	2014	16	4	7.9	lin	✓	8	8	28.5	lin	✗	128	8	16.8	lin	✓
Skylake	2015	16	4	9.0	lin	✓	8	8	2.0	lin	✗	128	12	212.0	XOR-7	✓
BroadwellXeon	2016	16	4	8.0	lin	✓	8	8	18.2	lin	✗	256	6	272.4	XOR-8	✓
Coffeelake	2017	16	4	9.1	lin	✓	8	8	26.3	lin	✗	128	12	230.3	XOR-7	✓

TLBLEED: TLB AS SHARED STATE

- We find more TLB properties
- Size, structure, sharing, miss penalty, hash function

		L1 dTLB					L1 iTLB					L2 sTLB				
Name	year	set	w	pn	hsh	shr	set	w	pn	hsh	shr	set	w	pn	hsh	shr
Sandybridge	2011	16	4	7.0	lin	✓	16	4	50.0	lin	✗	128	4	16.3	lin	✓
Ivybridge	2012	16	4	7.1	lin	✓	16	4	49.4	lin	✗	128	4	18.0	lin	✓
Haswell	2013	16	4	8.0	lin	✓	8	8	27.4	lin	✗	128	8	17.1	lin	✓
HaswellXeon	2014	16	4	7.9	lin	✓	8	8	28.5	lin	✗	128	8	16.8	lin	✓
Skylake	2015	16	4	9.0	lin	✓	8	8	2.0	lin	✗	128	12	212.0	XOR-7	✓
BroadwellXeon	2016	16	4	8.0	lin	✓	8	8	18.2	lin	✗	256	6	272.4	XOR-8	✓
Coffeelake	2017	16	4	9.1	lin	✓	8	8	26.3	lin	✗	128	12	230.3	XOR-7	✓

TLBLEED: TLB AS SHARED STATE

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- Map many virtual addresses to same physical page

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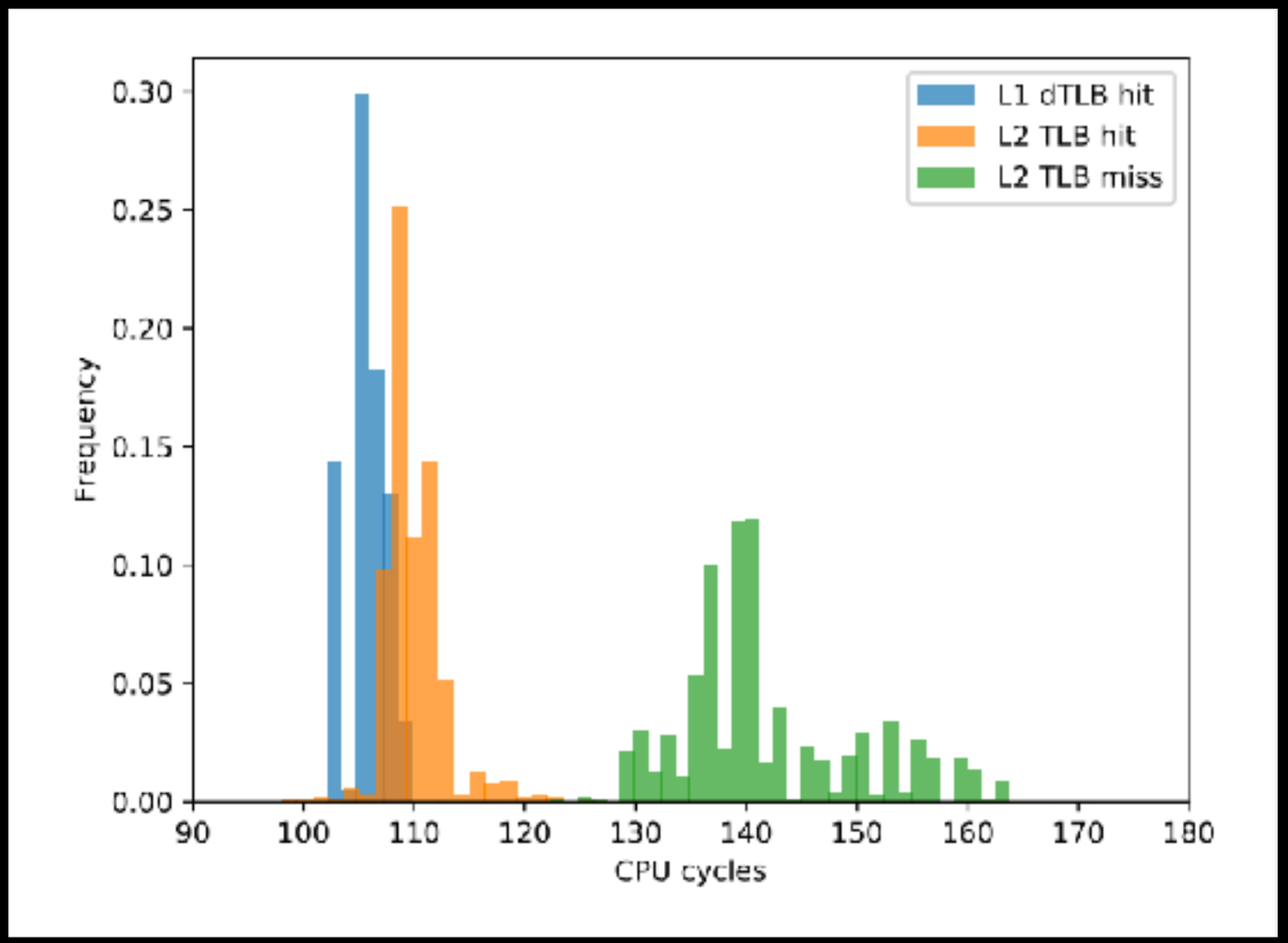

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- Let’s observe EdDSA ECC key multiplication

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 for (j=nbits-1; j >= 0; j--) {
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- Like RSA square-and-multiply
- But: we can not use code information! Only data..!

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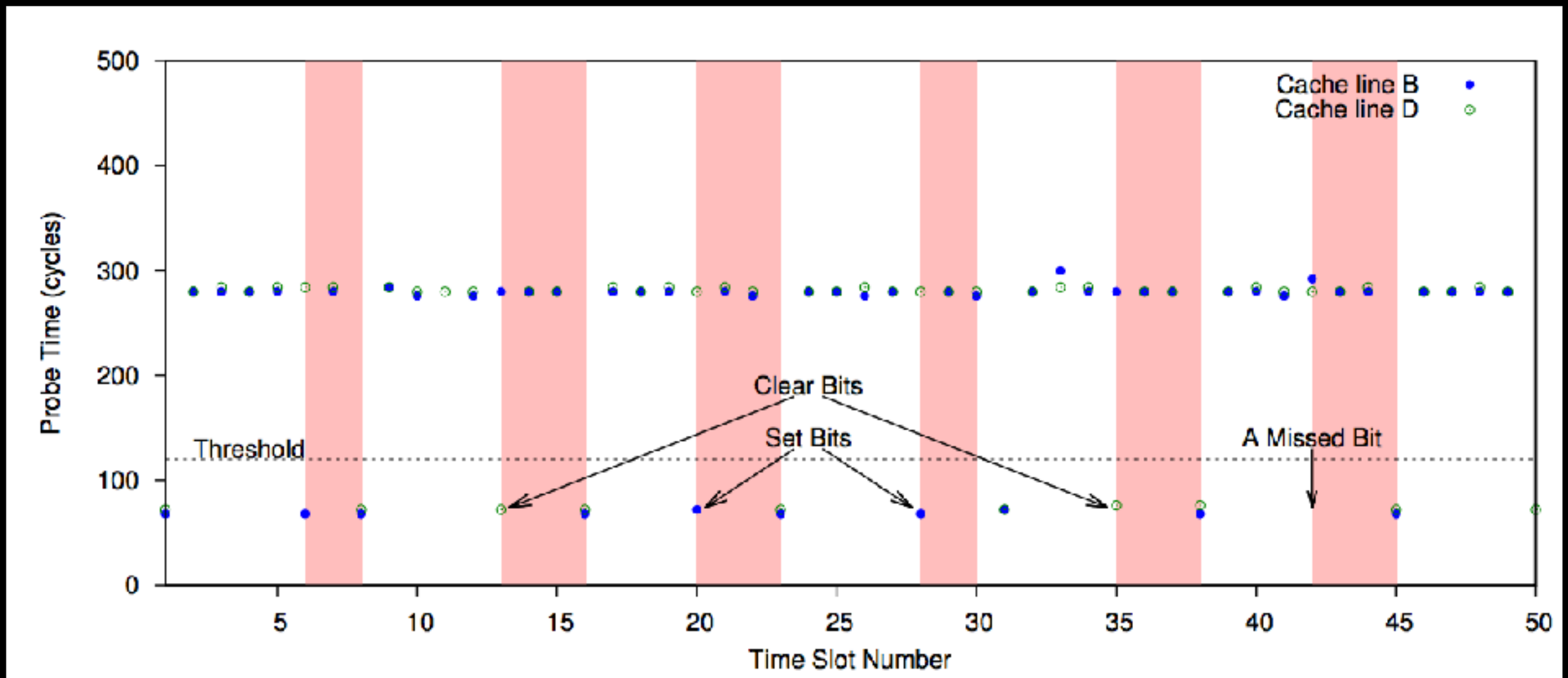

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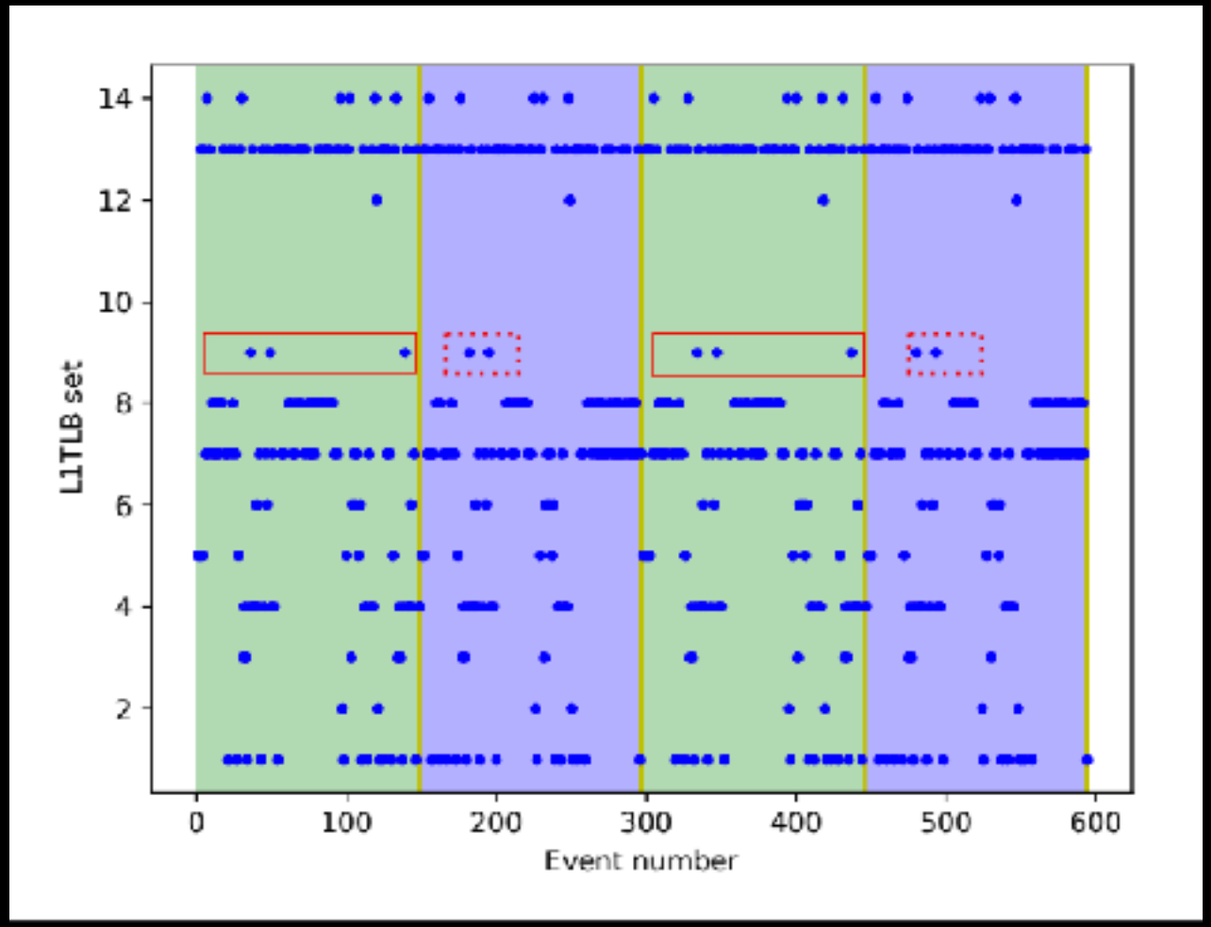

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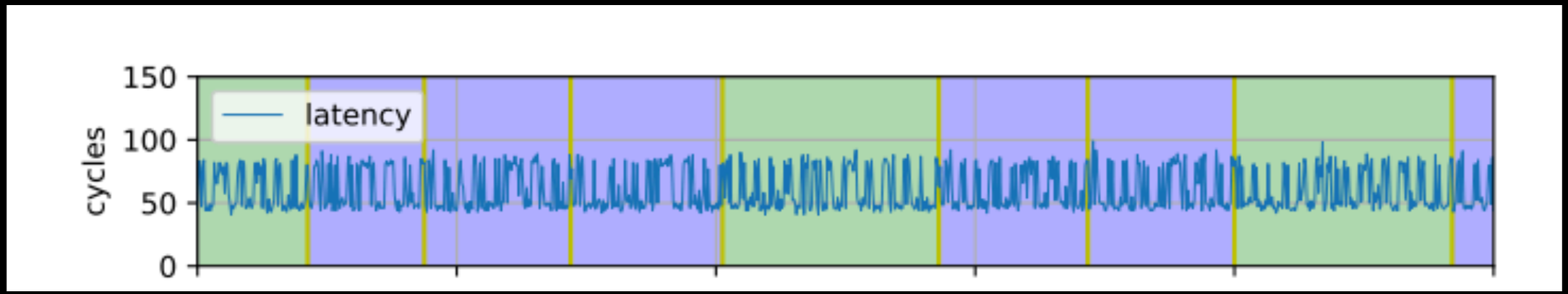

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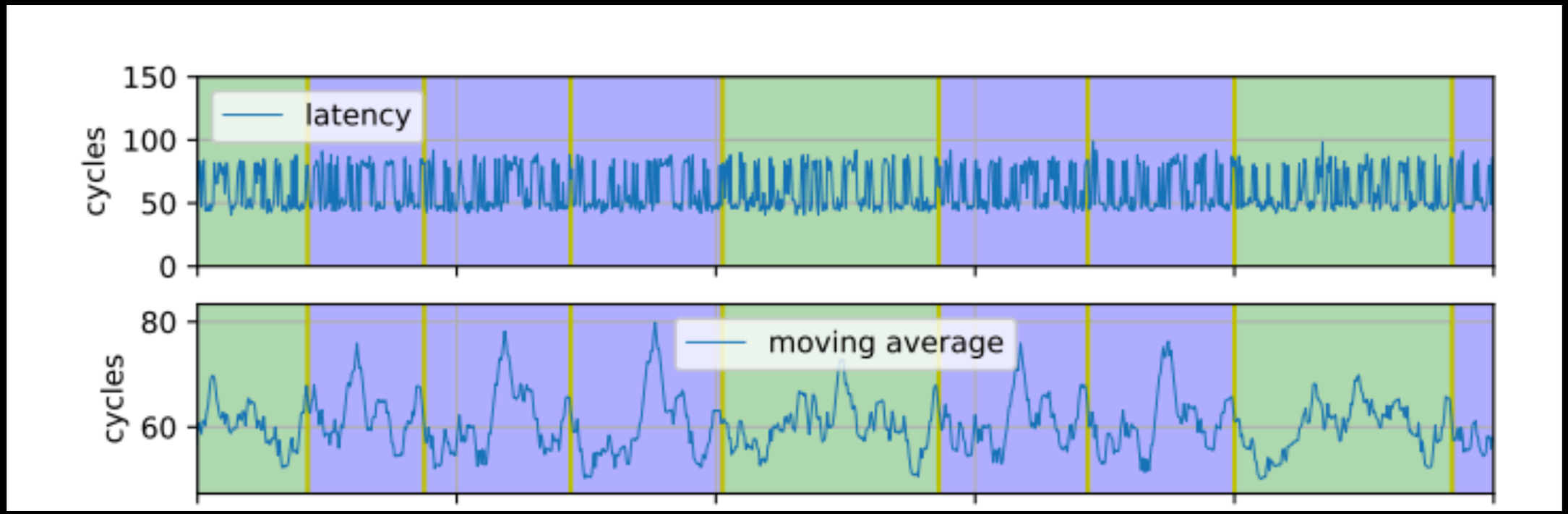

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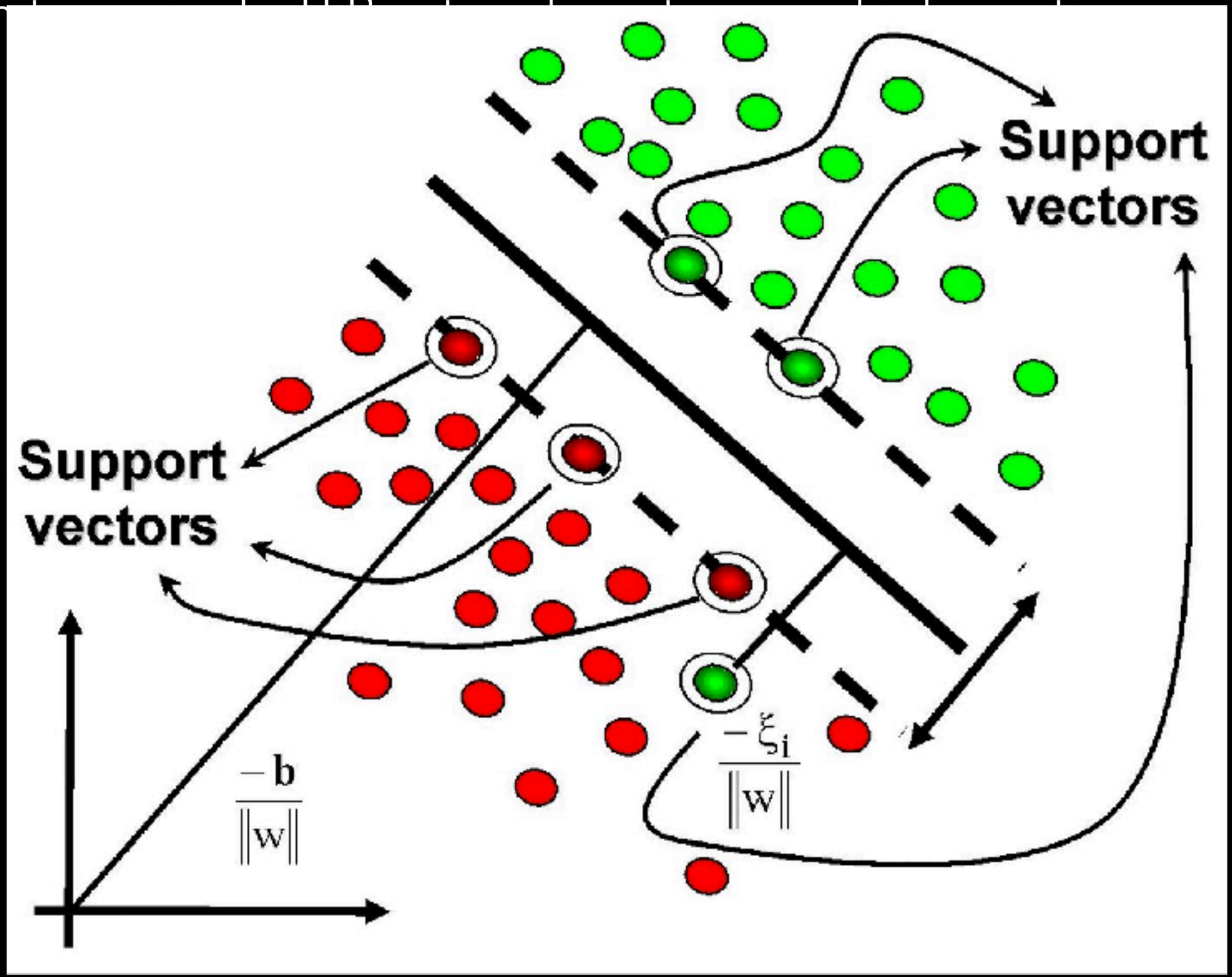

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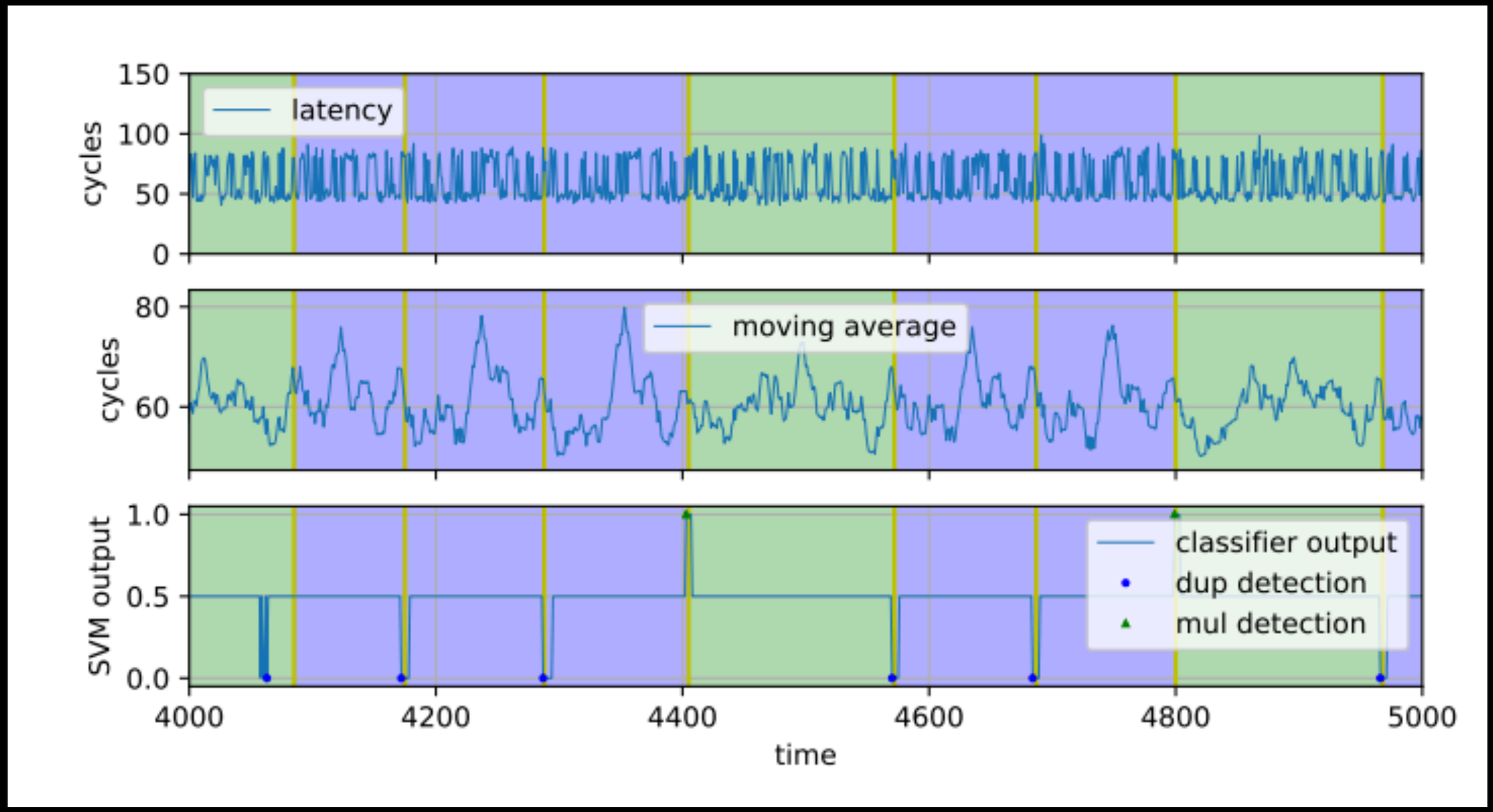

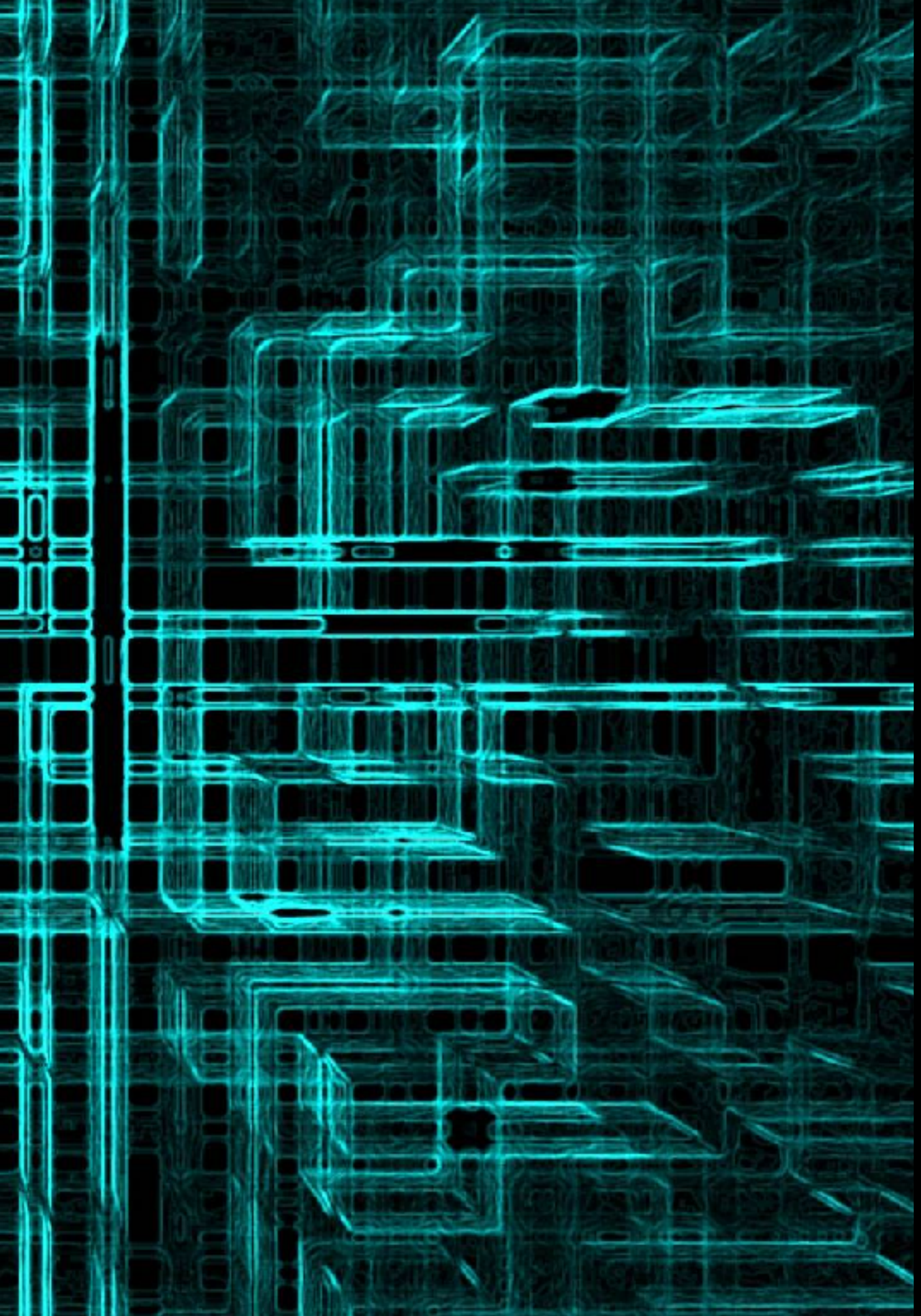

EVALUATION

TLBLEED RELIABILITY

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Microarchitecture	Trials	Success	Median BF
Skylake	500	0.998	$2^{1.6}$
Broadwell	500	0.982	$2^{3.0}$
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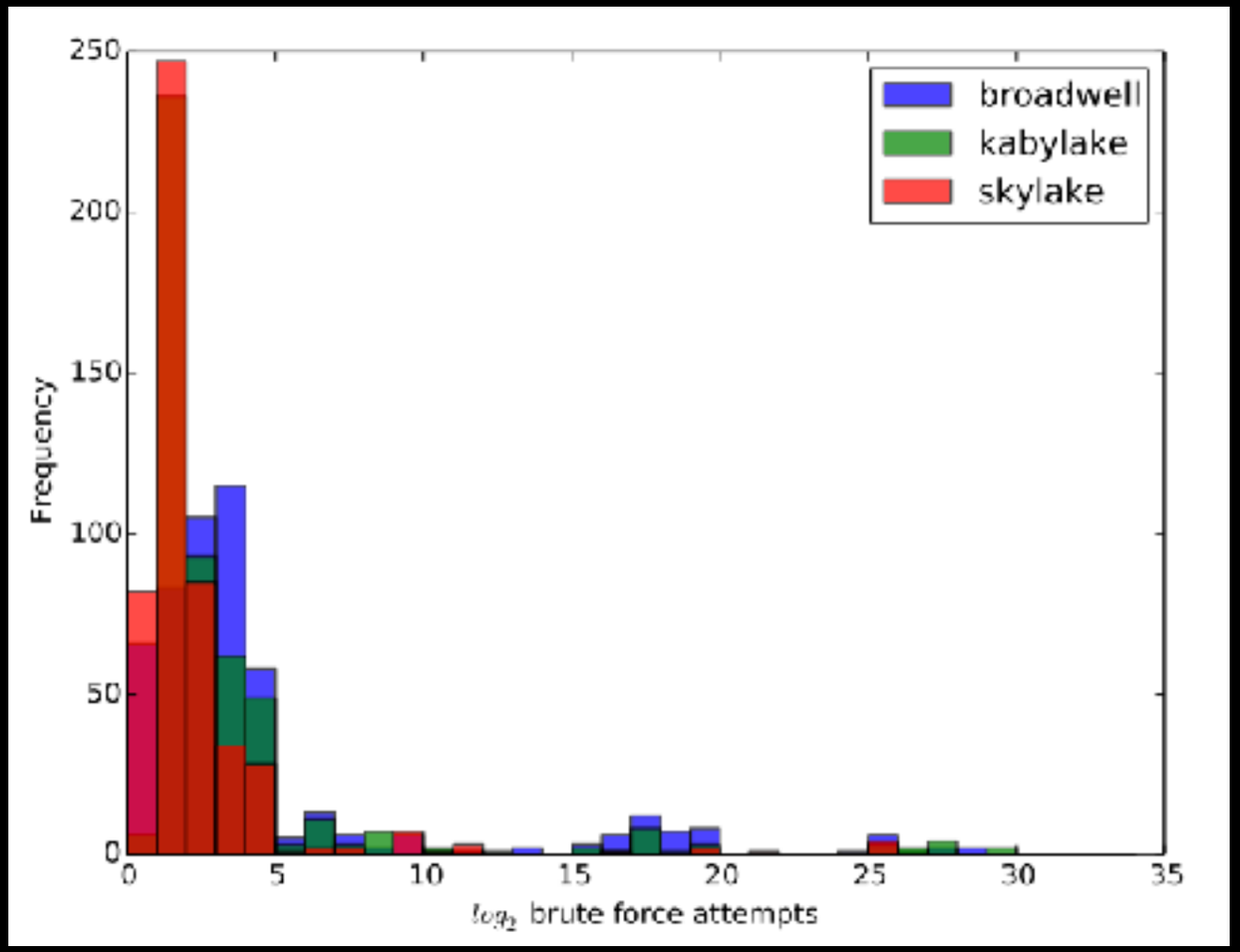

CREDIT

- Work also by Kaveh Razavi, Cristiano Giuffrida, Herbert Bos
- Some diagrams in these slides were taken from other work: FLUSH+RELOAD, Prefetch, DRAMA
- Yuval Yarom, Katrina Falkner, Peter Peßl, Daniel Gruss

CONCLUSION

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- Thank you for listening